

0.4177 24.6548 -110.2826 0.3787
0.5395 25.9683 -110.2540 0.3787
0.6968 25.4154 -110.2540 0.3787
0.9000 25.2939 -110.2541 0.3787

6. References

1. J. C. Candy, B. A. Wooley, and O. J. Benjamin. "A Voiceband Codec with Digital Filtering." *IEEE Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation*. Ed. J. C. Candy and G. C. Temes. 1992. PP. 385 - 399.
2. T. Karema, T. Ritoniemi, and H. Tenhunen. "An Oversampled Sigma-Delta A/D Converter Circuit using Two-Stage Fourth Order Modulator." *IEEE Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation*. Ed. J. C. Candy and G. C. Temes. 1992. PP. 322 - 325.
3. S. R. Norsworthy, R. Schreier, and G. C. Temes. *Delta-Sigma Data Converters: Theory, Design, and Simulation*. IEEE Press, 1997.
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5. D. R. Welland, et al. "A Stereo 16-Bit Delta-Sigma A/D Converter for Digital Audio." *IEEE Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation*. Ed. J. C. Candy and G. C. Temes. 1992. PP. 365 - 374.

The the maximum peak-to-peak magnitude of input signal is 0.8 V. Any value above will destabilize the system.

Figure 7 shows both the signal at AAF output , Which is smooth, and the signal at the decimation filter output, which has 16-bit resolution.

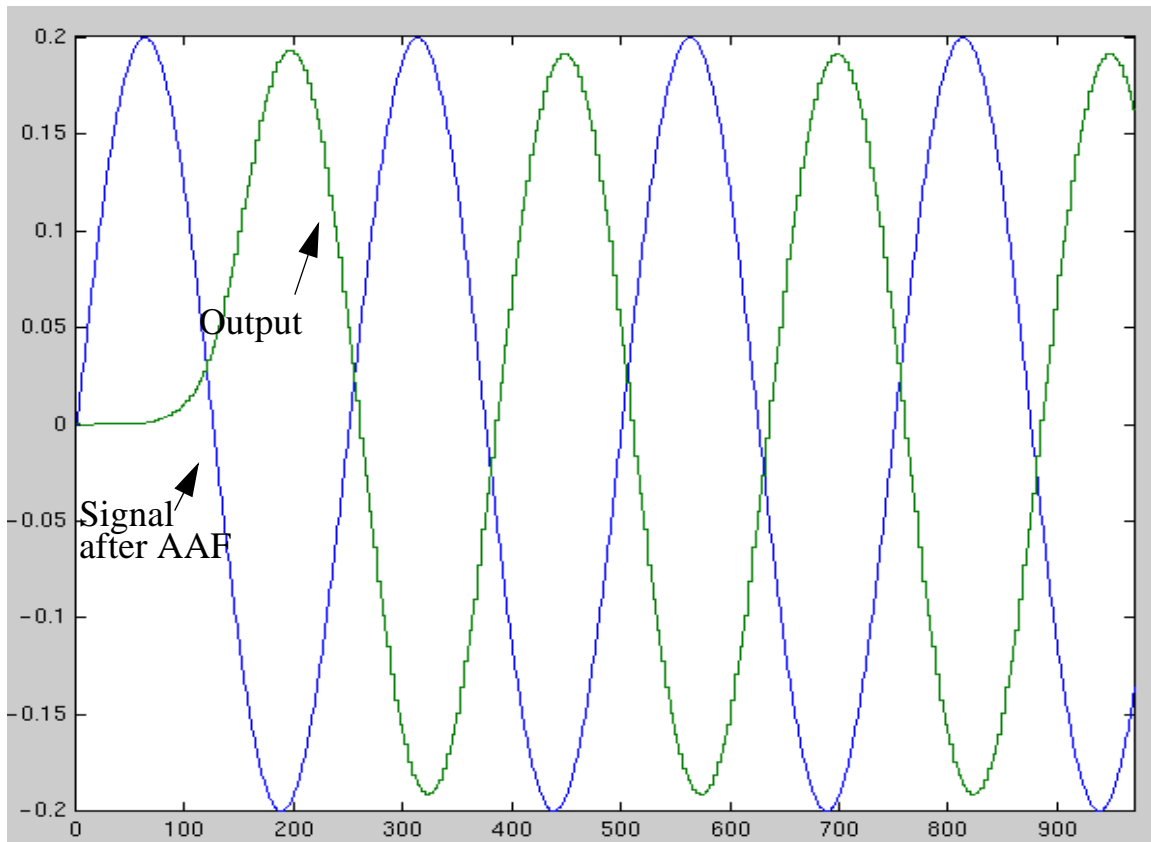


Figure 7: Output After Decimation Filter

The ideal signal to quantization noise ratio is 161 dB. But the peak SQNR is about $(24 + 110) = 124$ dB. The dynamic range is $(120 - 3) = 117$ dB.

A	SIGNAL	NOISE	Max(Dec_out)
0.0900	-62.0861	-133.6106	0.0804
0.1162	-59.7826	-131.4036	0.1039
0.1501	-57.7364	-129.7333	0.1341
0.1939	-55.4638	-127.0965	0.1732
0.2504	-53.2891	-124.8622	0.2237
0.3234	24.4170	-110.2541	0.3787

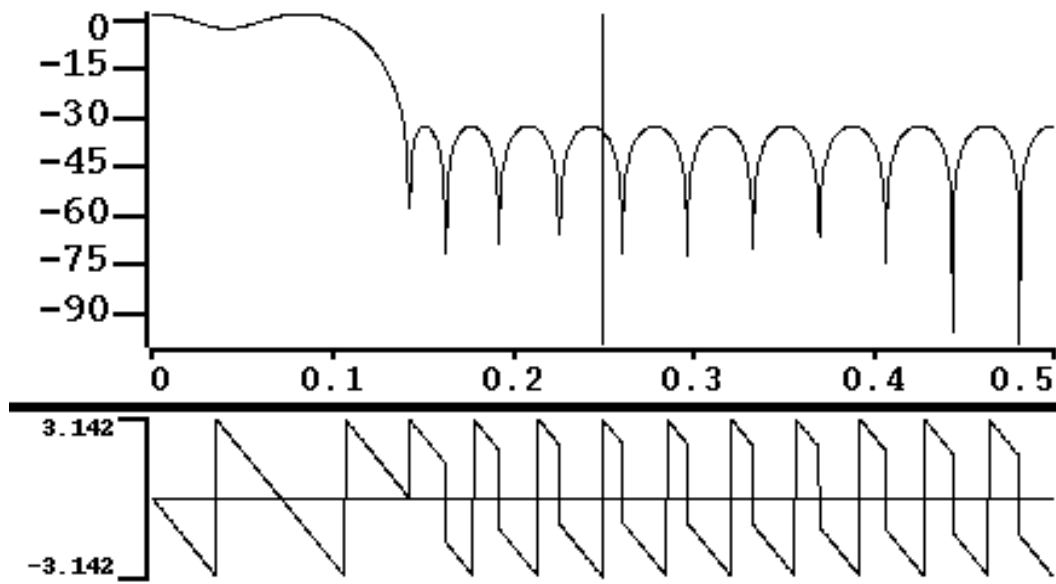


Figure 6: Magnitude and Phase of 2nd Stage Decimation Filter

$f_p = 0.11$; $f_s = 0.14$; $R_p = 3$; $R_s = 32$;

Coefficients of FIR transfer function:

$b = [-0.00010366 \ 0.02568 \ 0.036558 \ 0.046984 \ 0.044636 \ 0.025977 \ -0.0050503 \ -$
 $0.036724 \ -0.052988 \ -0.040025 \ 0.0068879 \ 0.079656 \ 0.15873 \ 0.21972 \ 0.24261$
 $0.21972 \ 0.15873 \ 0.079656 \ 0.0068879 \ -0.040025 \ -0.052988 \ -0.036724 \ -0.005050$
 $0.025977 \ 0.044636 \ 0.046987 \ 0.036558 \ 0.025681 \ -0.00010366]$

4. Anti-Aliasing Filter

Since the sampling frequency is much larger than the passband, the requirement for the anti-aliasing filter is relaxed. The transfer function for the filter is:

$$H(s) = \frac{0.5012}{s^2 + 0.6449s + 0.7079}$$

The transfer function can be implemented by a Sally-Key biquards filter. After AAF, the signal amplitude is only half of the input.

5. Simulation Result

3. Decimation Filter

The 4th order sigma-delta module is followed by decimation filter. The decimation filter reduces the sampling frequency from 1024 KHz to a lower value. This decimation filter has two stages.

3.1 First Stage of Decimation Filter

The first stage of the decimation filter is a 5th order FIR filter. It lowers the sampling frequency from 1024 KHz to 32 KHz. The transfer function is shown as:

$$H1(z) = \frac{1}{32^5} \left(\frac{1 - z^{-32}}{1 - z^{-1}} \right)^5$$

There are various methods that can be used to implement this transfer function. Running-sum architecture seems to be a good choice. The details of this architecture is described in [2]. One of the advantages of using running-sum architecture is that decimeter contains no multipliers, so few data memory locations are required.

3.2 Second Stage of Decimation Filter

The second stage of decimation filter lowers the sampling frequency from 32 KHz to 8 KHz. There are two options to implement this stage: FIR or IIR filter. FIR filter has linear phase and inherently stable, but the hardware is more complex than IIR filter. IIR can be implemented by cascading several biquards, but it has non-linear phase and also potentially unstable. To design a stable IIR is usually not an easy task.

To achieve 32 dB [1] attenuation at 4KHz, the order of equal ripple FIR is 29, and the order of elliptic IIR is 4. If the A/D is used for voice band coder, in which signal phase distortion is not an important issue, IIR filter may be good enough. For audio applications, FIR should be used to achieve high linearity.

FIR filter is considered here because of its linear phase. The coefficients of FIR filter was found by SPW software package. Figure below shown its magnitude and phase plots.

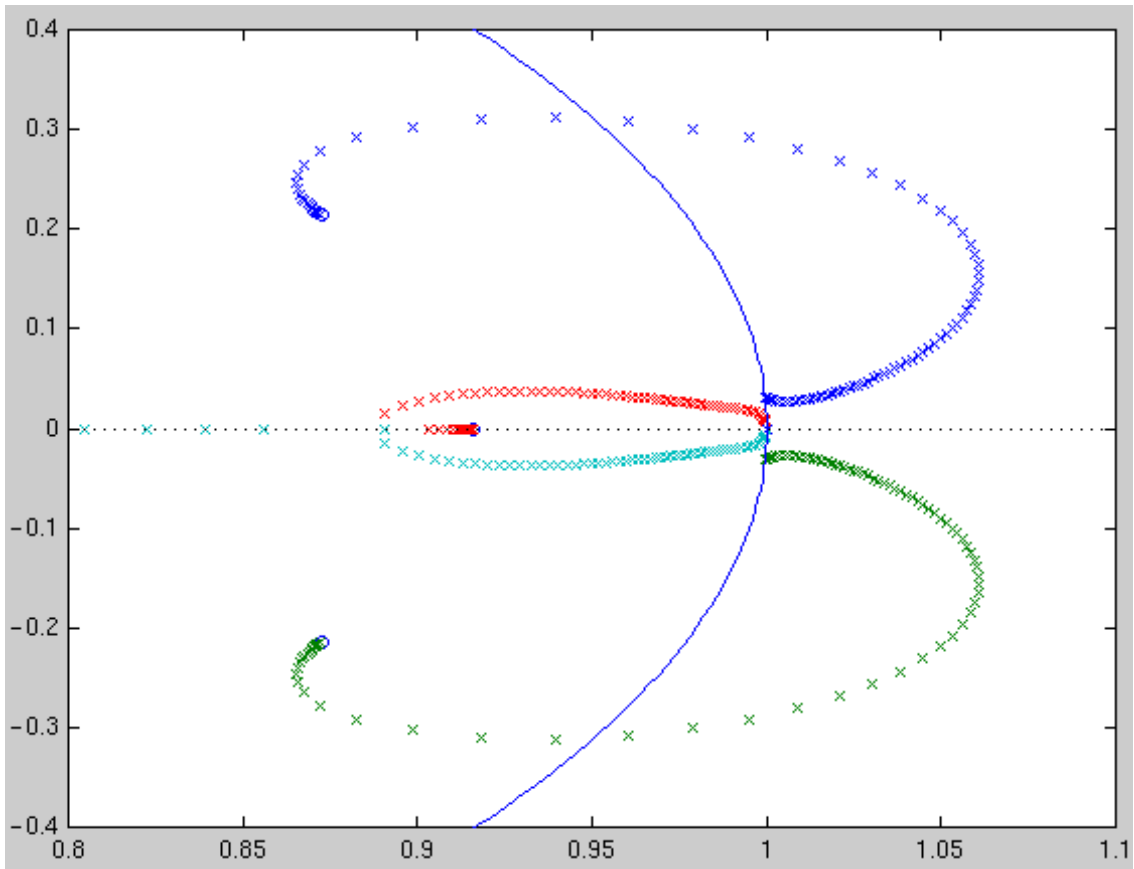


Figure 3: Root-Locus of the 4th Order Module

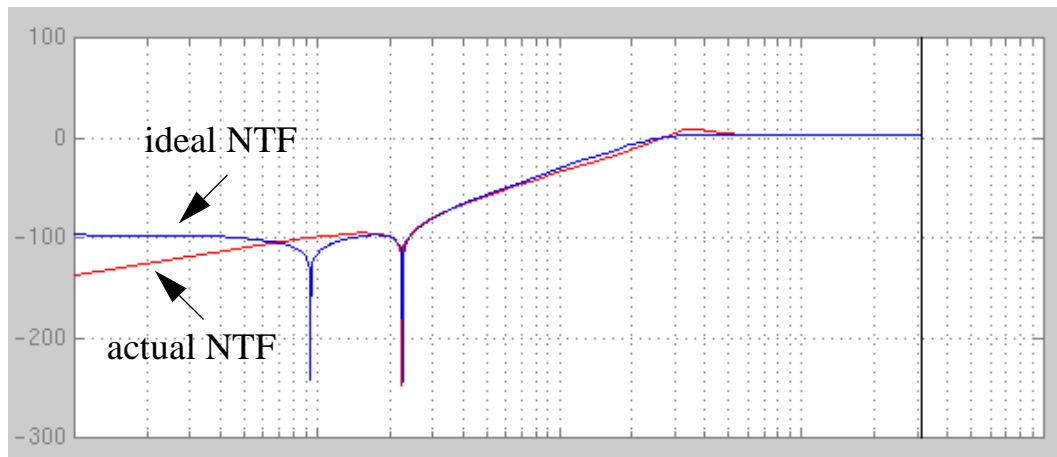


Figure 4: Noise Transfer Function

each integrator and each coefficient is adjusted. The final sigma-delta module is shown in figure 2.

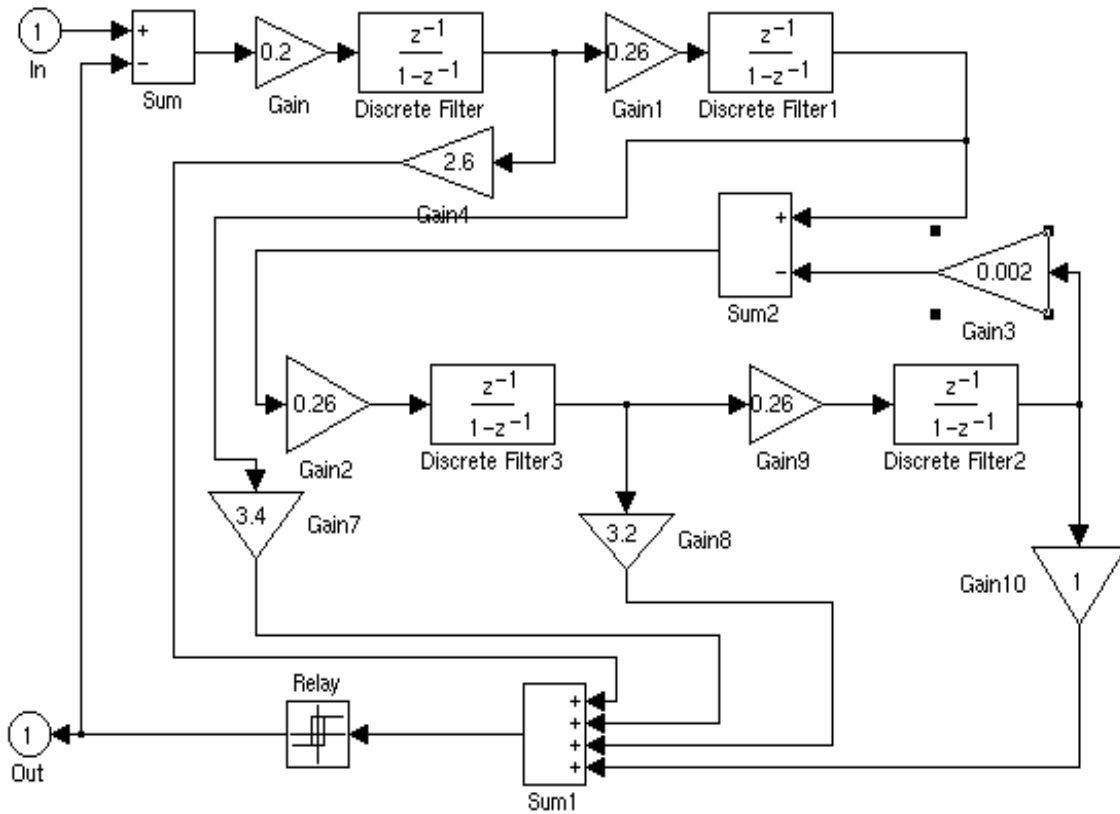


Figure 2: Diagram of 4th Order Sigma-Delta Module

The NTF and STF calculated from the module shown above:

$$NTF = \frac{1 - 3.9995 z^{-1} + 5.999 z^{-2} - 3.9995 z^{-3} + z^{-4}}{1 - 3.324 z^{-1} + 4.202 z^{-2} - 2.375 z^{-3} + 0.5011 z^{-4}}$$

$$STF = \frac{0.675 z^{-1} - 1.797 z^{-2} + 1.624 z^{-3} - 0.4989 z^{-4}}{1 - 3.9995 z^{-1} + 5.999 z^{-2} - 3.9995 z^{-3} + z^{-4}}$$

Root-locus diagram of the module and NTF are shown in figure 3 and figure 4.

In figure 1, feedforward coefficients, a_1 , a_2 , a_3 , and a_4 determine the poles of NTF. The zero of NTF is determined by feedback term, b_1 , which moves zero away from DC so that infinite noise attenuation is shifted away from DC to finite, positive frequencies. The stability of the module is controlled by NTF pole and zero locations and individual integrator gain. The transfer function of the last pair of integrators with feedback b_1 is derived as [3]:

$$\frac{Y}{X} = \frac{z}{z^2 - (2 - b_1)z + 1}$$

Usually, b_1 is a very small value [3]. So, poles can be adjusted without considering b_1 term.

With 128 oversampling ratio, 4th order Chebychev I high pass filter gives 100dB ideal stopband attenuation.

The ideal NTF and STF is shown as:

$$\text{NTF} = \frac{1 - 3.999 z^{-1} + 5.999 z^{-2} - 3.999 z^{-3} + z^{-4}}{1 - 3.327 z^{-1} + 4.2 z^{-2} - 2.378 z^{-3} + 0.5091 z^{-4}}$$

$$\text{STF} = \frac{0.6719 z^{-1} - 1.799 z^{-2} + 1.621 z^{-3} - 0.4909 z^{-4}}{1 - 3.999 z^{-1} + 5.999 z^{-2} - 3.999 z^{-3} + z^{-4}}$$

The ideal NTF shows that feedback coefficient b_1 , which is determined by numerator coefficients, is a very small value, so it can be ignored when calculate feedforward weights a_1 , a_2 , a_3 , and a_4 .

The values of a_1 , a_2 , a_3 , and a_4 are obtained from derived NTF. The calculation is done with Matlab code.

$$a_4 = 0.6730, a_3 = 0.2190, a_2 = 0.0410, a_1 = 0.0041, b_1 = 0.0005$$

In order to get reasonable capacitor values and to obtain a stable system, the gain of

Abstract

A fourth order sigma-delta ADC with a fifth order decimation filter is presented in this project. The oversampling rate is 128, the sampling frequency is 1024kHz, and the passband frequency is 3.6 KHz.

1. Introduction

In practice, second order sigma-delta module with IIR filter in the 2nd stage of decimation filter is the most popular architecture for voice coder. The advantage of this architecture is that it occupies less area and design is simpler; however, the dynamic range that can be achieved by a 2nd order sigma-delta ADC is usually around 80 dB.

In order to achieve higher dynamic range, a higher order sigma-delta ADC may be one of the options.

A fourth order modulator and a fifth order decimation filter presented in this project is to improve dynamic range to 90 dB. The first stage decimation filter lower the sampling frequency from 1024KHz to 32KHz. The second stage decimation filter lower the sampling frequency to 8KHz. The oversampling ratio is 128.

2. Oversampling Sigma-Delta Module

2.1 Architecture of Sigma-Delta Module

There are several topologies that may be used to implement the fourth order modulator. 1. Weighted feedforward summation,. 2. Feedforward summation with local resonator feedbacks. 3. Distributed feedback. 4. Distributed feedback with distributed feedforward inputs. 5. Distributed feedback with feedforward and local resonator feedbacks [3].

Weighted feedforward summation can be only used to implement Butterworth filters because stopband zeroes cannot be realized by this structure.

The architecture with distributed feedback, structure 3, usually requires larger capacitors, and it consumes more power than the feedforward summation topology.

A Fourth Order Sigma-Delta ADC

by

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