

A Power-Optimized CMOS Baseband Channel Filter and ADC for Cordless Applications

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Abstract

A 3.3V continuous-time anti-aliasing filter, 8th-order switched-capacitor channel filter and 10-bit ADC implemented in 0.6 micron CMOS for baseband channel filtering in direct conversion cordless phone receivers realizes an overall gain of 50dB with 42dB of gain control range. Dynamic range of the combined filter section is 87dB, and the maximum SNDR of ADC is 54dB at 40MS/s. Total power dissipation of 48mW¹ for both filters and ADC is achieved at 3.3 volts through optimum capacitor scaling in filter and pipeline ADC implementation.

Introduction

Two key objectives in the development of integrated circuits for RF communications receivers are the realization of higher levels of integration and the realization of receivers that are adaptable to more than one RF communication standard[1]. Toward this end, much recent work in integrated circuits for cordless phone and wireless LAN applications has focussed on various types of direct conversion architectures[4][5]. In this type of architecture, most of the channel select filtering can be implemented at baseband using a combination of on-chip continuous-time filter, switched capacitor filter, and digital signal processing. This allows both a higher integration level and easier adaptability to multiple standards of operation. A key problem in the implementation of such circuits is to achieve sufficiently low levels of power dissipation in the baseband filtering and signal processing circuits at the relatively high value of dynamic range required on a 3.3 volt supply. Since the composite baseband signal coming from the mixer in a direct conversion receiver contains

energy from all of the channels within the approximately 20MHz band passed by the RF filter, exceptionally large dynamic range and an exceptionally low noise level are required.

This paper describes a baseband signal processing system consisting of a continuous-time lowpass filter, a 6th-order lowpass switched-capacitor filter, a 2nd-order phase compensation filter, and a 10-bit pipeline A/D converter. This particular baseband system was intended for cordless phones and wireless LANs in general, and is optimized for the DECT cordless phone system. The overall power dissipation has been optimized by appropriate scaling of capacitor sizes through the stages of the filter as allowed by increasing signal amplitudes as adjacent channel energy is filtered out. Power is optimized in the ADC by using capacitor scaling as described in an earlier paper[2]. All switched capacitor circuitry uses bootstrapped clocks to allow operation of full-swing switched capacitor integrators and gain blocks on a 3 volt supply in a standard technology.

Baseband Building Blocks

Baseband circuits in a direct conversion receiver can be implemented with an continuous-time anti-aliasing filter and a switched capacitor filter followed by an ADC for backend digital signal processing as shown in figure 1. The continuous-time anti-aliasing filter performs coarse filtering of out-of-DECT band signals, and the switched capacitor filter which follows performs channel selection by filtering out nearby adjacent channels. The continuous-time filter is implemented with a 2x gain block and a Sallen-Key 2nd-order filter with a -3dB bandwidth of 1.5MHz. The 2x gain block is implemented using a simple differential amplifier with resistors. An extra R-C section is inserted between 2x gain block and the Sallen-Key section in order to obtain further rejection at the sampling frequency of the switched capacitor filter for anti-aliasing filtering. Continuous-time filter sections are implemented with two identical stages in parallel for a differential signal path. The switched-capacitor filter is implemented with three biquads followed by another biquad for phase compensation. The combined transfer function has a -3dB bandwidth of 700kHz and group delay distortion less than +/-75nsec sampling at 31.1MS/s. Sampling capacitors are implemented in binary weighted arrays with switches to achieve 42dB of digitally controlled gain with 6dB steps[3]. Finally, a 10bit pipeline ADC converter can be used for digitization of switched capacitor filter output for DSP. A 10 bit resolution on ADC is not normally required for many digital communication applications, but it was used here to ease requirements on gain function in the analog circuits with potential advantages on initial signal acquisition and AGC control. The ADC decimates the switched capacitor filter output by 3 sampling at 10.37M/s, which is 9 times the data rate(1.152Mb/s) for DECT.

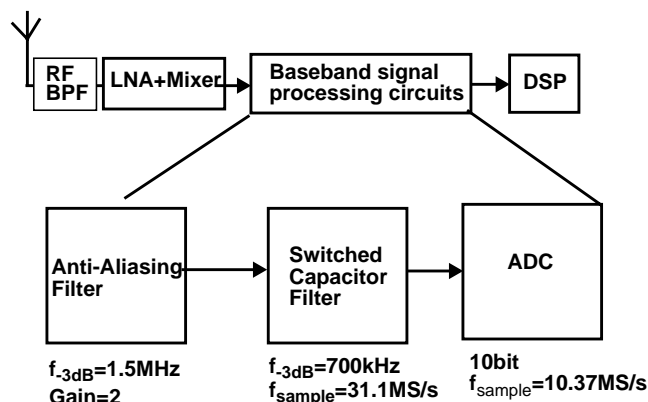


Figure 1. Baseband signal processing circuits for direct conversion receiver

1. 38mW measured for filter sections + 10mW projected for ADC sampling at 10MS/s. See experimental result section.

Low Voltage Implementation

Key elements in implementing above blocks are low voltage op amp for Sallen-Key section, high speed opamp for switched capacitor sections, and ADC with bootstrapped clock. A simple differential pair with source-followers for DC level shifting is used to implement a low output impedance op amp used for Sallen-Key section. Also, a low-voltage op-amp in [2] is used to implement the switched-capacitor integrator and the residue amplifier in each pipeline ADC stage. The op-amp topology is a two-stage configuration with a low-gain first stage to increase the effective transconductance of the amplifier for high speed operation. At low voltage operation, MOS transmission gates have high switch resistance due to insufficient gate voltage drive. A clock bootstrapping technique shown in figure 2 is used[2]. By applying the input clock signal of 3.3V, C1 and C2 are self-charged to 3.3V, and an inverted square wave output of ~5V is generated. This output clock of ~5V is then used to provide enough gate voltage to turn on transmission gates. In both switched-capacitor filter and ADC, only NMOS's are used for sampling switches due to a low signal common-mode voltage.

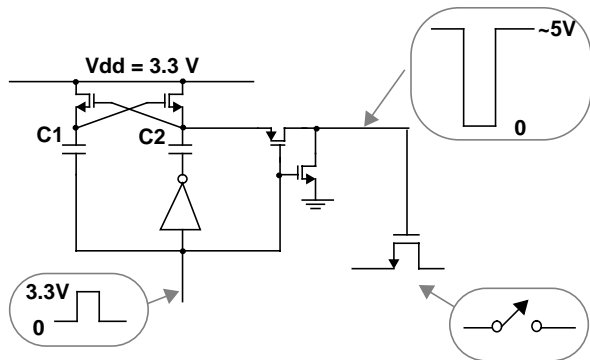


Figure 2. A bootstrapped clock generator for NMOS only switch

Experimental Results

Experimental prototypes were fabricated using 0.6um double-poly triple-metal CMOS technology. The third layer of metal was mainly used for routings of power supply lines to output pads. Separate prototypes for filter section and ADC were fabricated for testing purpose. However, it is also integrated as a part of larger system as shown in figure 3. Typical combined frequency response of the continuous-time anti-aliasing filter and switched capacitor is shown in figure 4. Input-referred RMS noise voltage of the combined filter sec-

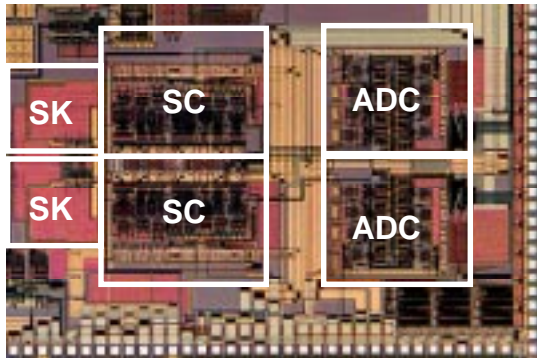


Figure 3. Die photo of the baseband circuits in a larger system

tion at maximum gain setting is 30uV, and the measured dynamic range is 87dB. For ADC, the maximum sampling rate is 40MS/s with power dissipation of 28mW. Power dissipation much less than 10mW is projected at 10MS/s by reducing the op amp bias current. The maximum SNDR of the ADC is 54dB with 100kHz input at the maximum sampling rate. Key performances are summarized in Table 1 and Table 2.

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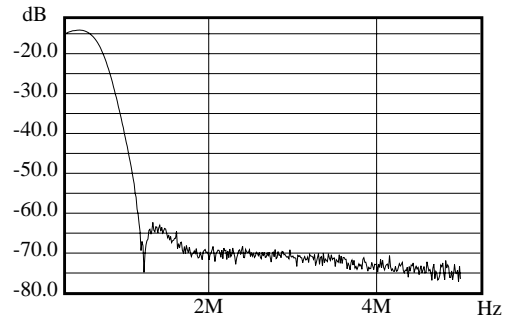


Figure 4. Typical frequency response of the combined filter section with the gain set at 32dB and 47dB input signal attenuator.

Table 1: Performance summary for filter section

Die Size(Active area)	2.4 x 1.2 mm ²
Power dissipation	38mW @31.1MS/s
Dynamic range	87dB
Gain control range	42dB@6dB steps
Group delay distortion in passband	Group Delay Distortion < +/- 75nsec

Table 2: Performance summary for ADC

Die Size(Active area)	1.2 x 1.2 mm ²
Power dissipation	28mW@40MS/s < 10mW ^a @10MS/s
SNDR	54dB with 100kHz input sine wave

a. projected power dissipation

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