
Appendix B

MOS Sampling Circuits

B.1 Introduction

For any A/D converters, the first thing that the converters need to do is to sample the time varying input signal. In CMOS technology, sampling is generally done with a MOS switch and a sampling capacitor. This circuit function, like every other circuit blocks on the chip, is not ideal. Various sources of errors are associated with it. In this section, a brief discussion of three major sources of nonidealities is presented with reference for a full discussion to several Ph.D. theses in the research group. [12][14]

B.2 Finite Bandwidth

Figure 1 shows a simplest sample-and-hold circuit implemented with a MOS switch and a sampling capacitor. When the MOS switch is on, an on-resistance is associated with the switch depending on the switch size and gate drive. The on-resistance and the sampling capacitor form a RC time constant which defines the bandwidth. The -3dB frequency is given by

$$f_{-3dB} = \frac{1}{2\pi R_{sw} C_s} = \frac{1}{2\pi} \times \frac{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)}{C_s} \text{ where}$$

$$R_{sw} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t) \text{ and } V_{ds} \text{ is small.}$$

For a given switch size and fixed supply voltage, the -3dB frequency increases as the technology improves (increased C_{ox}). With scaled technology (reduced L), the -3dB frequency also increases. However, the -3dB frequency is also directly proportional the supply voltage. Therefore, reducing the supply voltage to be compatible with digital circuits and lower the power also degrades the input bandwidth of SC circuits.

In summary, to achieve high input bandwidth for a fixed sampling capacitor, the on-resistance needs to be small by increasing C_{ox} and reducing L. Although increasing W can also decrease the on-resistance of the switch, the added parasitic capacitance will cancel the effect. With the ongoing trend of low voltage, low power can only be achieved at the expense of input bandwidth.

B.3 Charge Injection

Figure 2 shows a MOS switch and a sampling capacitor. When the switch is on, the voltage across the sampling capacitor tracks the time-varying input signal within the bandwidth. Some charges are present in the MOS channel, this is a result of forming a conducting channel under the MOS gate. The charge in the channel is on the order of $C_{ox}(V_{gs} - V_t)$. When the switch is turned off, charges either flow to the input source or to the sampling capacitor and create a small $\Delta V = \frac{\Delta Q}{C_s}$. ΔQ is a function of several parameters which include input impedance, source impedance, clock falling edge, etc. To the first order, 50% distribution between the input source and C_s can be assumed.

Charge injection is also a function of input voltage ($C_{ox}(V_g - V_{in} - V_t)$) and needs to be treated carefully to avoid signal dependent distortion. It has been shown that adding a dummy switch at half the size of the sampling switch can cancel the charge injection error to the first order. The dummy switch is driven by the inverse clock which will absorb the charge injected from the sam-

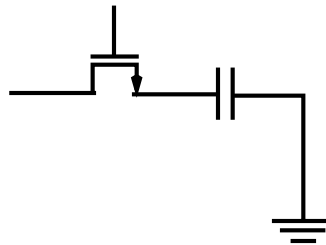


Figure B.1 A Simple Sample-and-Hold Circuit

pling switch instead of being added onto the sampling capacitor. This technique works the best when the clock edge is sharp which means a rough 50% distribution between the input source and sampling capacitor can be assumed. However, an absolute matching between transistors is required for this technique and impedance on both sides need to be roughly equal. For a low impedance input source, this is generally not possible.

Figure 2 shows a technique generally known as bottom plate sampling. This technique requires an additional switch, M2, which defines the sampling instance by turning off before M1. Since the switch M2 is always connected to the input common mode (AC ground), the charge injection is a constant. Therefore, we have eliminated the signal dependence in M2 charge injection. However, charge injection still occurs when M1 goes off. Since the sampling capacitor is floating at this point, the extra charge added onto the capacitor will be shorted to ground when M3 is on during the charge transfer phase in SC circuit.

Charge injection on a sample-and-hold circuit is a signal dependent error, which is really difficult to deal with. Special technique by adding an extra dummy switch can cancel the error to the first order. In differential circuit, the use of bottom plate sampling which results a common mode charge injection can be used.

B.4 Clock Feedthrough

Ideally, when the clock edges are switching, this will not affect the operation of SC circuit. However, due to some parasitic capacitance associated with the MOS switches, the voltage difference in clock switching may be coupled into the sampled input and create an error.

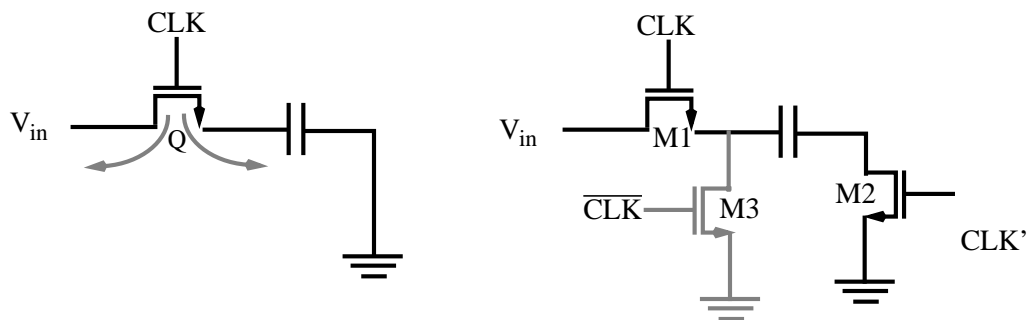


Figure B.2 Sample-and-Hold with Bottom Plate Sampling

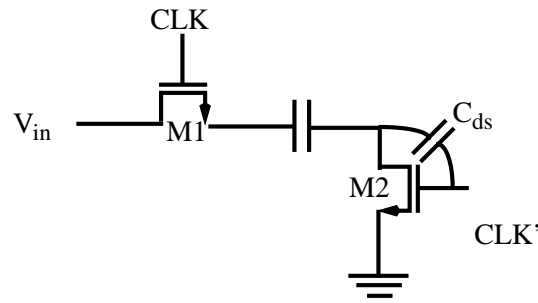


Figure B.3 Illustration for Clock Feedthrough

Figure 3 shows a typical sample-and-hold circuit employing the bottom plate sampling described in the previous section. C_{ds} is the overlapping capacitance between the gate and drain of the MOS switch. When the clock voltage on the gate switches between high and low, this voltage drop is coupled into the signal via the capacitor divider.

The clock feedthrough can be corrected to the first order by using a differential signal path. As long as the error is present on both signal inputs and the same magnitude, it can be cancelled by taking the input differentially. However, this technique, once again, depends on the absolute matching of transistors.

It will be shown later that these errors are carefully examined for the prototype and techniques mentioned above are used to correct these errors.