

# **A 1.9GHz Wide-Band IF Double Conversion CMOS Integrated Receiver for Cordless Telephone Applications**

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Rapid growth in the portable communications market has pushed designers to seek low-cost, low-power, highly integrated solutions for the RF transceiver. A number of recent efforts have concentrated on integrating many of the discrete radio receiver components in a low-cost silicon process such as CMOS [1][2]. This paper describes a prototype of a monolithic CMOS receiver that combines RF and baseband functionality by taking the carrier signal at the LNA input and producing a 10-bit digital baseband waveform. A Wide-Band Intermediate Frequency Double Conversion (WBIFDC) architecture is utilized to remove the need for external narrow-band IF filters.

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The experimental chip includes a LNA, a new image-rejection mixer, and two baseband signal processing paths, each of which includes a 2<sup>nd</sup>-order Sallen & Key anti-alias filter, an 8<sup>th</sup>-order switched capacitor filter and a 10-bit pipelined ADC. The receiver was designed to meet the specifications of the Digitally Enhanced Cordless Telephone (DECT) standard. The device achieves an overall receiver reference sensitivity of -90dBm, an input IP3 of -7dBm, with an overall power dissipation of 198mW from a 3.3V supply. The design was fabricated in a 0.6 $\mu$ m double-poly, triple-metal TSMC process.

The wide-band IF double conversion architecture (Figure 1) modulates all of the RF spectrum passing through the RF filter directly to baseband in its entirety where channel selection is done by low-pass signal processing as in the case of direct conversion. No band-pass filtering is performed at the IF frequency, in this case 190MHz. However, in contrast to direct conversion, the translation takes place in two steps, using two oscillators and two sets of mixers. This provides two principal advantages over direct conversion systems: no oscillator operates at the RF input frequency, and the tuning of the receiver can be accomplished using the second low-frequency LO. Because the first LO is fixed, easier trade-offs may be obtained with regard to LO phase noise. As in the case of direct conversion, channel selection can be performed at baseband, where digitally-programmable filter implementations can potentially enable more multi-standard capable receiver features.

To reduce the effects of high frequency coupling, the entire analog RF and baseband signal paths are fully differential. The ADC output drivers are realized with differential source coupled buffers which reduce digital substrate

coupling effects into the analog section of the chip. Further isolation is provided by numerous substrate contacts, guard rings and on-chip bypass capacitors.

The low  $f_t$  and  $g_m/I_d$  ratio of CMOS devices limit the performance of traditional broadband LNA designs. Therefore, a tuned narrow-band technique is used to passively enhance the voltage gain of the LNA and perform impedance matching [3]. This approach relaxes the conventional trade-off between noise figure and power dissipation and allows linearity to be traded for noise figure. The LNA was implemented as a single stage differential common source amplifier with on-chip spiral inductors (Figure 2). The LNA input network utilizes bondwire inductor L1 and spiral inductor L2 to enhance the Q of the input network in addition to performing impedance matching. Spiral inductor L3 tunes the output node while improving both the gain and the image rejection for the overall receiver.

Similar to conventional heterodyne systems, the wide-band IF double conversion architecture retains the need for image rejection. In the DECT standard, approximately 80dB of rejection is required in the image-band (which lies 380MHz below the carrier). The image rejection is accomplished through a combination of the front-end external RF filter, the tuned LNA, and a new image-rejection technique achieved by the double-conversion configuration. This scheme utilizes both the in-phase and quadrature-phase of the local oscillators to realize a broadband image reject function. At the LNA output, a complex modulation from RF to IF is performed (Figure 1). Then, the IF signals are mixed to baseband where in-phase and quadrature channels are generated from both of the I&Q IF channels. By properly combining these four baseband signal paths, the correct phase can be obtained for constructive interference of signals above

the first local oscillator frequency, while to first-order any received RF signals below the first LO are cancelled. Passive components typically used to realize conventional image-rejection mixer schemes have been eliminated from the signal path. The magnitude of image rejection is limited by gain matching of the mixer paths and by LO deviation from quadrature. To mitigate the effects of both low frequency noise at baseband and any DC components as a result of self mixing from IF to baseband, two offset cancellation current DACs are used at the output of the image-rejection mixer.

The individual mixer units are realized with a doubly-balanced CMOS version of the Gilbert Cell (Figure 3). The cascode devices M3 and M4 improve the isolation between the mixer LO and IF/RF input terminals. Current sources M11 and M12, along with a common-mode feedback loop comprised of M13, M14, and M15, set the output common-mode voltage. Two triode region PMOS devices, M9 and M10, determine both the loading and gain of the mixer cell. The conversion gain is adjustable from 0dB to 10dB by modulating the current through diode-connected device M16.

In the prototype receiver, 55dB overall image rejection was obtained from the receiver using externally supplied LOs with an on-chip phase shifting network adjusted for quadrature. The loss of the balun was estimated to be 2dB in the image-band while 8dB of rejection was contributed by the LNA, leaving approximately 45dB of image rejection from the mixer portion of the receiver. The receiver used in conjunction with an RF filter can easily achieve 80dB of overall image rejection.

More aggressive dynamic range requirements are placed on the baseband circuits because the IF filter has been removed in the WBIFDC radio architecture. After the mix from IF to baseband, a 2<sup>nd</sup>-order Sallen & Key filter performs anti-aliasing before subsequent sampling into an 8<sup>th</sup>-order switched capacitor filter. The filter is designed to meet the bandwidth requirements for a single DECT channel (-3dB frequency at 700kHz). In addition to providing channel filtering, variable gain is provided from 6dB to 48dB in 6dB increments. The baseband channel filter output is then sampled by a 10-bit pipelined 10MHz ADC. Capacitor scaling techniques were employed to optimize the filter and ADC stages for both noise and power. The implementation of these blocks has been described earlier [4].

The prototype device (Figure 5) was packaged using a Chip-On-Board technology. Both the die backside and the chip board landing zone were gold plated. The chip was attached to the board using a conductive epoxy with bondwires running from the chip pads directly to landing zones found on the board. Single-ended to differential conversion was achieved using an external balun placed in front of the LNA and LO input ports. Experimental results are shown in Tables 1 and 2. The receiver reference sensitivity of -90dBm was obtained by measuring the ADC output signal-to-noise ratio; 10dB of SNR was assumed to meet the DECT BER requirement of  $10^{-3}$ . A 3<sup>rd</sup>-order intermodulation intercept point of -7dBm referred to the LNA input was obtained (Figure 4).

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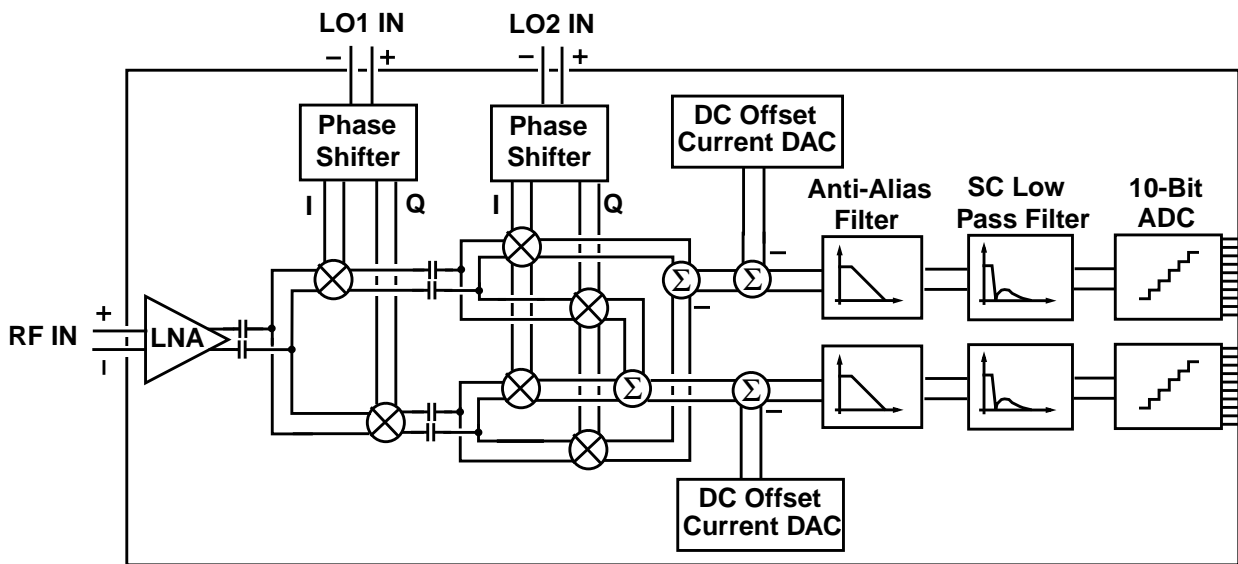


Figure 1: Wide-band IF double conversion receiver architecture.

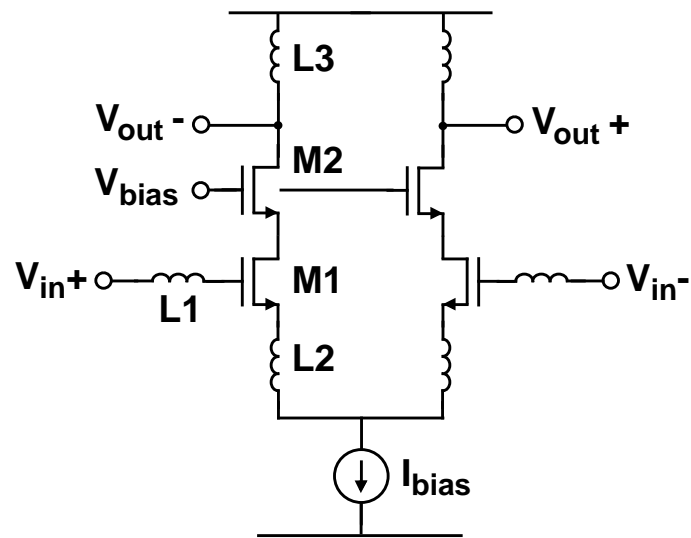


Figure 2: Narrow-band inductively tuned LNA.

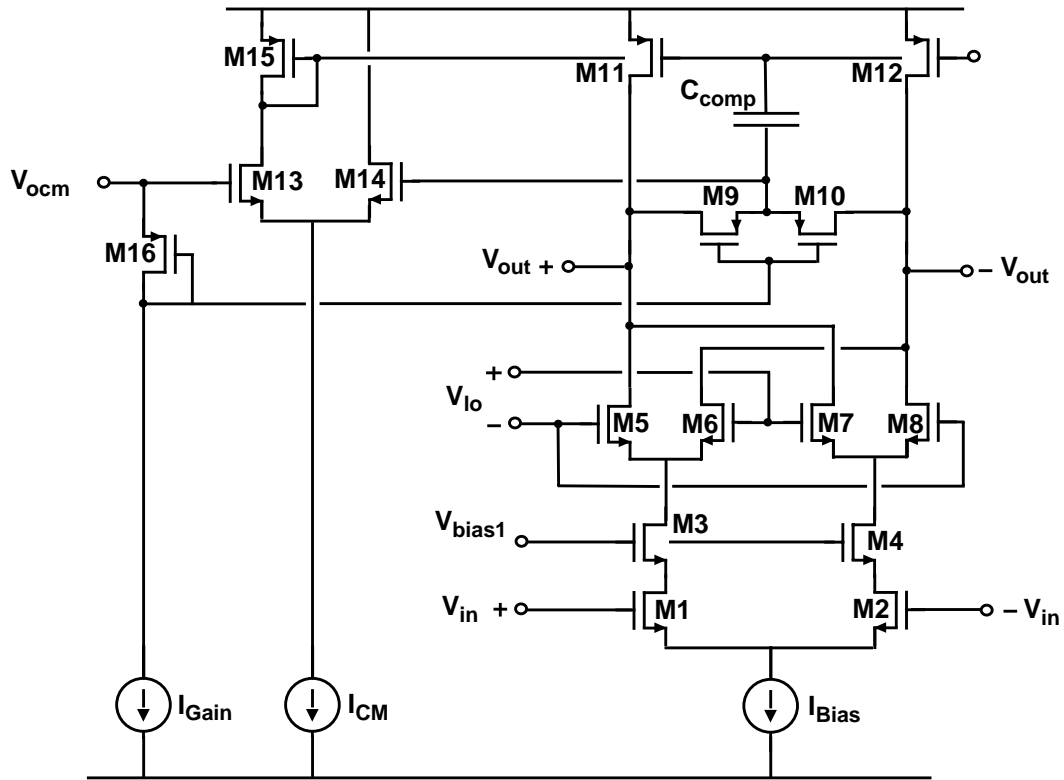


Figure 3: Variable gain active mixer with common-mode feedback.

Sensitivity	-90 dBm*
Input IP3	-7 dBm**
Receiver Image Rejection	55 dB
$P_{ob3dB}$ (Max. gain setting)	-33 dBm***
$P_{-1dB}$ (Min. gain setting)	-24 dBm
Max. Receiver Gain	78 dB
Min. Receiver Gain	26 dB
Supply Voltage	3.3 V
LO1	1.7 GHz
LO2	182 - 197 MHz
Carrier Frequency	1.882 - 1.897 GHz
Active Chip Area (including bias)	15 mm <sup>2</sup>

**Table 1: Receiver performance features.**

\* -83dBm sensitivity required for DECT.

\*\* -27dBm input referred IP3 required for DECT.

\*\*\* Blocker 1 DECT channel from carrier.

LNA	41 mW
RF to IF Mixers	17 mW
IF to Baseband Mixers	34 mW
Baseband Filters	66 mW
ADCs	40 mW
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Total Chip	198 mW

**Table 2: Distribution of receiver power dissipation**

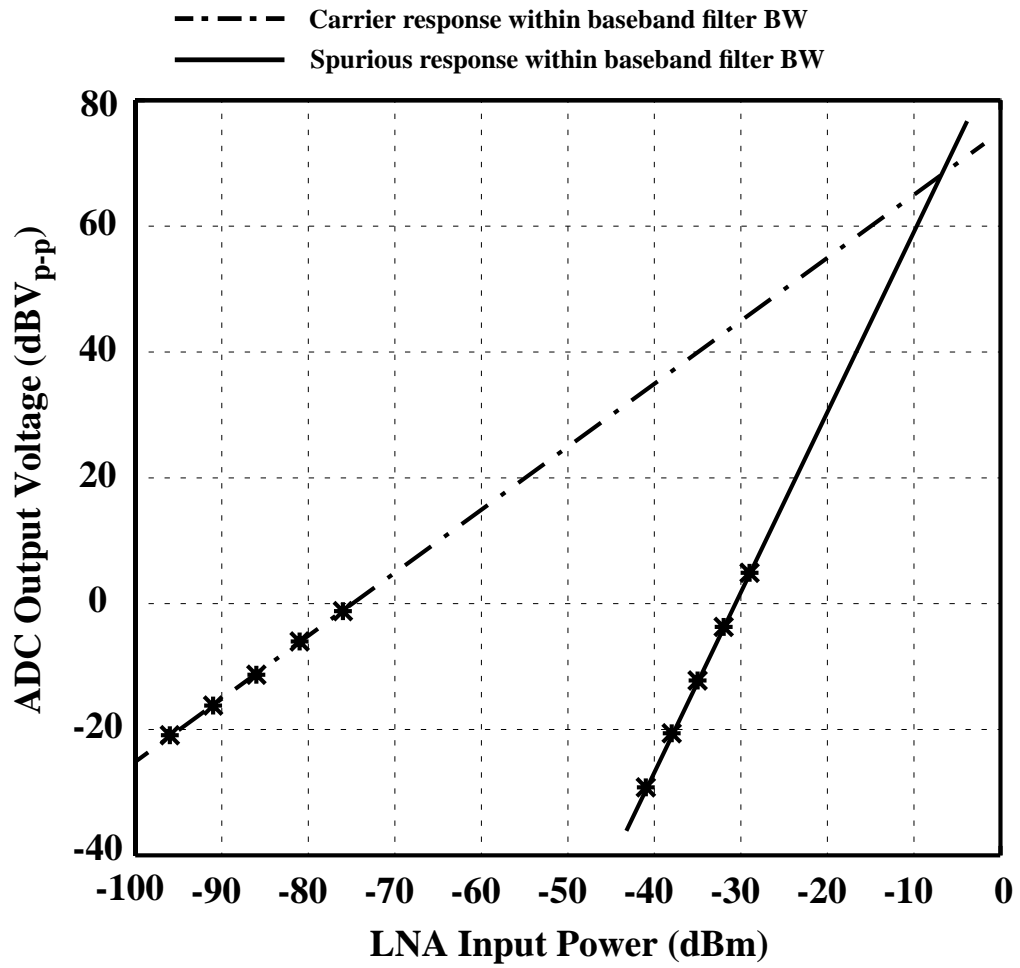


Figure 4: Receiver two-tone (spaced 2 & 4 DECT channels from carrier) test for 3<sup>rd</sup>-order intermodulation.

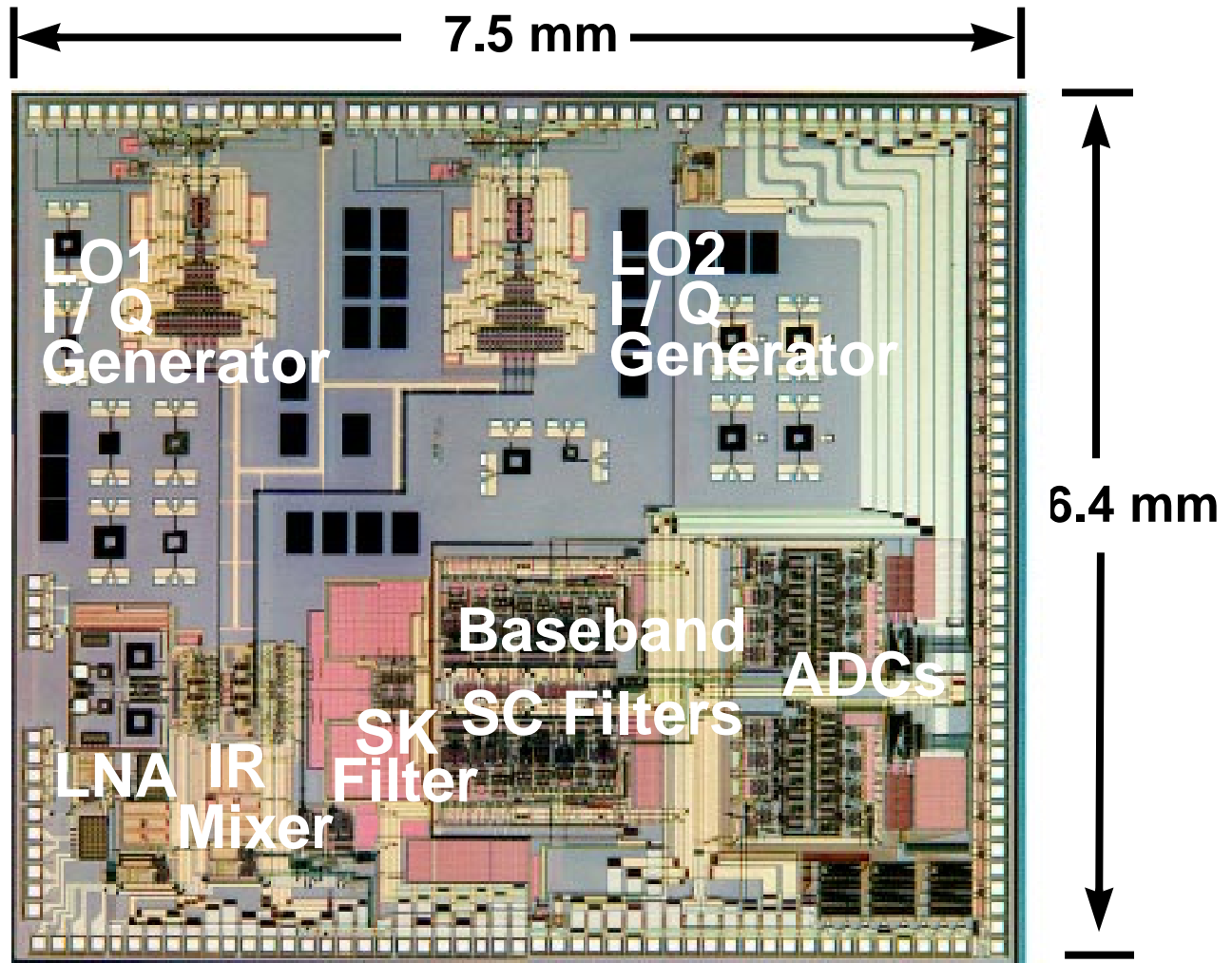


Figure 5: Receiver chip micrograph.