

CMOS VLSI Frequency Translation for Multi-Standard Wireless Communication Transceivers

Projections of world-wide cellular phones sales indicate a potential market growth from 50 millions units sold in 1996 to over 100 million by the year 2000 [1]. Similar explosive growth can be expected in the cordless telephone and Personal Communication Services (PCS) area. These devices all require low-cost, low-power, and small form factors for their transceiver units. Current transceiver implementations employ a collection of large discrete components which are highly cost and power inefficient. In addition, the transceiver is designed and manufactured for a specific application which targets a distinct cellular, cordless, or PCS standard. To address the goals of low-cost and low-power in a high volume environment we are currently working on a monolithic silicon solution for the transceiver in an inexpensive integrated circuit technology known as CMOS. To enhance portability, receiver systems are being explored which address a variety of standards. This fully integrated solution requires the exploration of both new receiver architectures and circuit design techniques.

This research project focuses on one of the key receiver blocks which performs a frequency translation, or shifting of the incoming RF spectrum to a lower frequency signal where signal processing can be applied before detection. This function is usually accomplished using what is commonly referred to as a mixer. The new receiver architecture under investigation emulates the traditional super-heterodyne approach in the sense that the rf signal spectrum is translated to baseband in a two step approach requiring an intermediate frequency. While mixing the carrier spectrum to an intermediate frequency (IF), an undesired spectrum equally distanced on the opposite side of the first Local Oscillator (LO) is also translated to the same frequency as the desired band, thus leading to the potential of signal corruption. This phenomenon is referred to as the image problem.

The super-heterodyne receiver requires expensive, discrete SAW filters to attenuate the signal power within the image-band. An additional discrete filter is then needed to address the issue of strong adjacent channel signals at IF. This project seeks to define a new

two step frequency translation circuit which performs image cancellation without the need for external filters. Previous attempts to eliminate the image-rejection filter include on-chip passive components to create a 90° phase shift. However, the attenuation band and the magnitude of the image-rejection are functions of the absolute value of passive components making it difficult to design and susceptible to wafer process variations. A new image-rejection mixer configuration utilizing six active mixers to perform the required attenuation in the image-band will be investigated in this work.

The hardware implementation of the active mixers is an adaptation of the original continuous time bipolar Gilbert cell which was selected because of the clear trade-offs between, signal gain, distortion, and power. This research seeks to understand the limitations of CMOS mixers in the context of a multi-standard environment. Issues with regard to conversion gain, distortion, noise, power, dynamic range and bandwidth are related to some of the current specifications for foreign and domestic, PCS, cellular and cordless telephone standards such as IS-54, DECT, GSM, and 802.11. A new adaptation of a CMOS gilbert cell will also be examined.

To demonstrate feasibility of concept, a prototype integrated circuit incorporating the entire receiver made to meet the specifications of the Digital European Cordless Telephone Standard was fabricated in a $0.6\mu\text{m}$ TSMC CMOS process. Measured results indicate a 26dB image attenuation relative to the carrier with a power consumption of 55mW.

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