

A 75mW 128MHz DS-CDMA Baseband Correlator for High-Speed Wireless Applications

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Abstract

A 5V DS-CDMA correlator uses sampled analog signal processing to achieve 75mW power dissipation, 128MS/s processing rate and 54dB input dynamic range in a 1.2um CMOS process. A new passive correlation technique eliminates the integrating opamp and associated power and settling time overhead. Six 64-chip correlators recover the 2Mb/s data stream from the doubly modulated (PN & Walsh) I & Q input signals. A 10bit 8MS/s ADC digitizes the outputs of the correlators for subsequent digital data processing and acquisition/tracking control.

Introduction

Direct Sequence Code Division Multiple Access (DS-CDMA) has been successfully applied to many low bandwidth wireless application (e.g., cellular phones [1] and GPS systems [2]). In these systems with modest speed requirements low-power high-resolution¹ analog-to-digital converters (ADC) can digitize the baseband signal directly allowing demodulation of the DS-CDMA signal in the digital domain. However in wideband DS-CDMA systems, such as wireless local area networks (LAN), higher processing speeds favor low-power high dynamic range implementations that involve demodulation using analog signal processing prior to digital conversion.

This paper describes a DS-CDMA baseband demodulating chip employing a new passive switched-capacitor structure as a correlator that minimizes power while permitting operation at 128MHz. The chip includes a low-power 10bit 8MS/s ADC [4] that provides a digital interface for both the data and synchronization signal paths.

The chip is intended to be part of a wireless LAN system [5] that is patterned after the QUALCOMM cellular phone system[1]. It uses Walsh function modulation as well as the normal pseudo-random noise (PN) sequence modulation to create a 64-dimensional code space that can accommodate up to 64 channels (users). One channel is reserved for sending an unmodulated PN signal (pilot tone) to aid synchronization.

1. The ability of a DS-CDMA receiver to reject undesired in-band signals, particularly narrow-band interferers [3], is closely linked to its input dynamic range. When an ADC directly samples a DS-CDMA signal its bit resolution determines the input dynamic range of the baseband system.

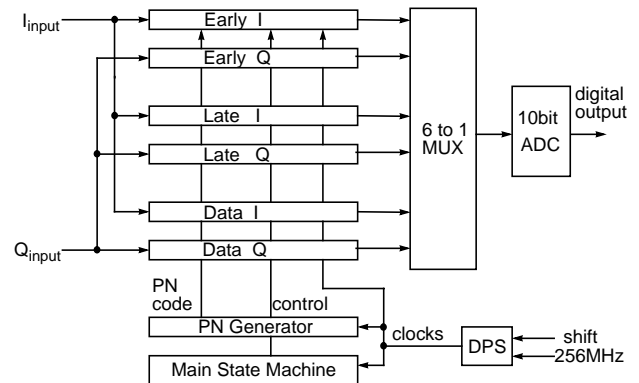


Fig. 1. DS-CDMA correlator block diagram

Chip Architecture

Fig. 1 is a block diagram of the DS-CDMA receiver. The differential I & Q inputs to the correlators are signals down-converted to baseband by a RF receiver [5]. Each I & Q data path is composed of 3 correlators; Early, Late, and Data. Acquisition and tracking synchronization uses the Early/Late correlator outputs and data demodulation uses the Data correlator output in the normal delay-locked loop configuration [2]. In this type of tracking loop, the Early/Late correlators sample their inputs in the opposite phase of the 64MHz system clock from the Data correlator which translates to an effective sample rate of 128MHz.

Each data bit is encoded as a sequence of 64 PN/Walsh bits (hereafter called chips) yielding an 18dB processing gain for the data path. Tracking & acquisition signals are generated by accumulating 14 Early/Late 64-chip correlations yielding a 30dB processing gain. This is done to make tracking & acquisition more robust.

A single ADC is multiplexed to digitize all 6 correlator outputs. A 16-stage linear feedback shift register [2] generates the PN code and a shift register chain allows off-chip programming of the Walsh code. 2 control inputs, one each for acquisition and tracking, feed a digital phase shifter (DPS) logic block to regulate phase slippage. The DPS operates at 256MHz provided by an off-chip clock source.

New Passive Correlator

The correlator implementation is key to the high-speed and low-power performance of this chip. Like most

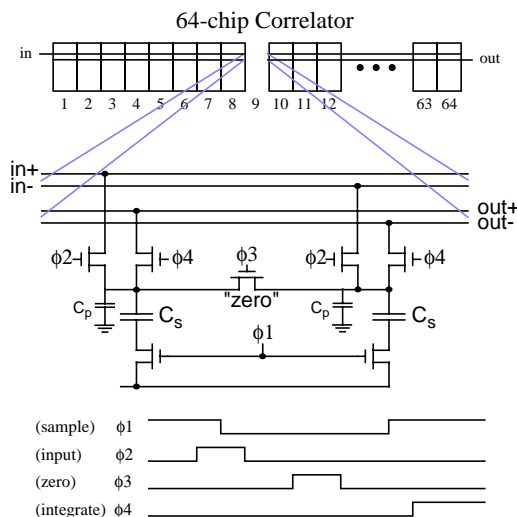


Fig. 2. Single differential sampling cell (1 of 64 per correlator)

switched capacitor (SC) integrator circuits, samples of the input signal are stored on capacitors. However, instead of integrating the charge on a separate integrating capacitor using an opamp the sampling capacitors themselves are tied together to integrate the charge. Thus the sampling capacitors double as integrating capacitors. Fig. 2 illustrates how the sampling cells of a correlator are interconnected in order to accomplish this.

By removing the opamp two advantages are realized. First, the settling time of the opamp is eliminated. Thus the operating speed is a function of the sampling time constant which is simply the on-resistance of the NMOS switch times the sampling capacitance. Second, the static power dissipation of the opamp is also eliminated.

However when using this passive technique two issues must be addressed. The first has to do with the charge injection deposited on the parasitic capacitances (C_p) of the sampling capacitor's (C_s) top-plate (normally removed by an opamp). This is addressed by momentarily turning on the "zero" switch at the appropriate time nulling out the charge injection error (see timing in Fig. 2).

The other issue is that the gain of the correlator is parasitic sensitive and thus inherently less than one. However the gain is constant and can be calibrated out if needed. In this DS-CDMA correlator application only relative gain is important so this was not a problem.

Experimental Results

Dynamic range measurements were performed with a single user signal + pilot tone of equal power. The maximum user input amplitude was 1.5V and the minimum was 3mV yielding a dynamic range of 54dB. Table I presents the key specifications.

The chip was fabricated in a standard 1.2um double metal

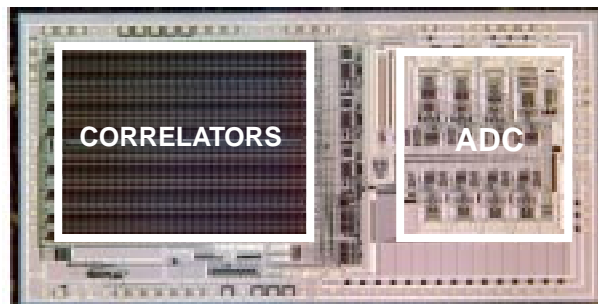


Fig. 3. Die photo of DS-CDMA baseband correlator

double poly CMOS process. Fig. 3 shows a microphotograph of the chip.

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Table I: Key Specifications

Power Supplies	3.3V (ADC), 5V(rest)
Data rate	2Mbits/s
Chip rate	64Mchips/s
Sampling rate	128MSamples/s
Power dissipation	75mW
Dynamic range	54dB
Die Size	4.5 mm x 9.3 mm

References

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