

Biography of PAUL R. GRAY

Paul R. Gray (S'65, M'69, SM'76, F'80) was born in Jonesboro, Arkansas, on December 8, 1942. He received the BS, MS, and PhD degrees from the University of Arizona, Tucson, Arizona, in 1963, 1965, and 1969, respectively.

In 1969 Professor Gray joined the Research and Development Laboratory, Fairchild Semiconductor, Palo Alto, California, where he was involved in the application of new technologies for analog integrated circuits, including power integrated circuits and data conversion circuits. In 1971 he joined the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley. His research interests during this period have included bipolar and MOS circuit design, electro thermal interactions in integrated circuits, device modeling, telecommunications circuits, and analog-digital interfaces in VLSI systems. Professor Gray is the co-author of a widely used college textbook on analog integrated circuits. During year-long industrial leaves of absence from Berkeley, he served as Project Manager for Telecommunications Filters at Intel Corporation, Santa Clara, CA, in 1977-78, and as Director of CMOS Design Engineering at Microlinear Corporation, San Jose, CA, in 1984-85.

Professor Gray has held a number of administrative posts at Berkeley, including Director of the Electronics Research Laboratory (1985-86), Vice-Chairman of the EECS Department for Computer Resources (1988-90), Chairman of the Department of Electrical Engineering and Computer Sciences (1990-93), Dean of the College of Engineering (1996-2000), and Executive Vice Chancellor and Provost, 2000-2006. He is currently Emeritus Professor of EECS, and holds the Andrew S. Grove Chair in Electrical Engineering

Professor Gray has been co-recipient of best-paper awards at the International Solid State Circuits Conference and the European Solid-State Circuits Conference, and was co-recipient of the IEEE R. W. G. Baker Prize in 1980, and the IEEE Morris K. Liebman award in 1983. . In 1994 he received the IEEE Solid-State Circuits award, and in 2004 the IEEE James H. Mulligan, Jr. Education Medal. He served as editor of the IEEE Journal of Solid State Circuits from 1977 through 1979, and as Program Chairman of the 1982 International Solid-State Circuits Conference. He served as President of the IEEE Solid-State Circuits Council from 1988 to 1990, and is a member of the National Academy of Engineering.

Professor Gray is married and has two sons.

PAUL R. GRAY

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Education

Ph.D. (7/69), M.S. (6/65), and B.S. (8/63) in Electrical Engineering, University of Arizona, Tucson, Arizona

Professional Experience

Member of technical staff, Semiconductor Division, Fairchild Camera and Instrument Corporation, June 1969 to August 1971, engaged in development of analog integrated circuits.

Visiting Lecturer, Electrical Engineering and Computer Sciences, University of California, Berkeley, September 1971 to July 1972.

Assistant Professor of Electrical Engineering and Computer Sciences, University of California, Berkeley, July 1972 to June 1974.

Associate Professor, Electrical Engineering and Computer Sciences, University of California, Berkeley, July 1974 to July 1978.

Project Manager, Telecommunication Filter Program, Intel Corporation, June 1977-June 1978.

Professor, Electrical Engineering and Computer Sciences, University of California, Berkeley, July 1978 to present.

Director, CMOS Product Development, Microlinear Corporation, June 1984-June 1985

Acting Director, Electronics Research Laboratory, College of Engineering, University of California, Berkeley, August 1985 to July 1986

Vice-Chairman, Electrical Engineering and Computer Sciences Department, 1988 to 1990

Chairman, Electrical Engineering and Computer Sciences Department, 1990 to 1993

Dean, College of Engineering, 1996-2000

Executive Vice Chancellor and Provost, 2000-2006

Consultant to numerous electronics companies, 1972-present.

Professional Activities

Editor, IEEE Journal of Solid State Circuits, 1977-1980

Associate Editor, IEEE Journal of Solid State Circuits, 1974-1977

Member, Program Committee, International Solid State Circuits Conference (1974, 1975, 1976, 1977, 1978, 1979, 1980, 1986, 1987)

Chairman, Program Committee, 1982 International Solid State Circuits Conference

Member, Board of Directors, Solid State Communications Inc., Hayward, California, 1973-1977

Member, IEEE Committee on Network Standards (1973, 1974)

IEEE Ad Hoc Visitor, Engineering Accreditation Commission (Accredits Engineering Schools). 1981-1985

Member, Program Committee, IEEE International Symposium on Circuits and Systems, (1984, 1985)

Vice-President, IEEE Solid State Circuits Council, 1985-1987

Member, Administrative Committee, IEEE Circuits and Systems Society, 1981-1984

Member, US Program Committee, VLSI Circuits Symposium, Tokyo, Japan (1987, 1988, 1989)

President, IEEE Solid-State Circuits Council, 1988, 1989

Member, Board of Directors, Microlinear Corporation, 1988-1991

Member, Board of Directors, Level One Communications, 1993 to 1999

Member, Board of Directors, Marvell Technology Group, 1999 to 2008

Member, Board of Directors, ASEE Engineering Dean's Council, January to July 2000

Member, Public Policy Committee, ASEE Engineering Dean's Council, January to July 2000

Member, General Electric Senior Research Awards Committee, ASEE, 2000

Member, School of Engineering Advisory Board, Stanford University, 1996-2000

Member, Engineering Advisory Board, University of Michigan, 1997-2000

Member, Action Forum on Diversity in the Engineering Workforce, 2000

Swiss Federal Institute of Technology (EPFL), Lecturer in RF Integrated Circuit Design short course, Lausanne, Switzerland, 2001, 2002, 2003, 2006, 2007

Member, Board of Directors, Telegent Systems, 2005 – present.

Member, SRC University Advisory Council, 2005-2008.

Chair, External Review Committee, Department of Electrical Engineering, Stanford University, December, 2006

Member, Board of Trustees, Gordon and Betty Moore Foundation, 2008- present

Councillor, National Academy of Engineering, June 2008 –present

Secretary-Treasurer, National Museum of Innovation in Science and Technology Consortium, 2008-present

Society Memberships

Sigma Xi
Eta Kappa Nu
IEEE (Fellow)
National Academy of Engineering

Awards and Honors

Outstanding Paper Award, 1975 International Solid State Circuits Conference (co-recipient)

Outstanding Paper Award, 1977 European Solid State Circuits Conference (co-recipient)

W. R. G. Baker Prize in 1980 for the best paper appearing in an IEEE Publication in 1980 (co-recipient)

IEEE Morris K. Liebmenn award, 1982
(Co-recipient on all of the above)

IEEE Centennial medal recipient (1984)

Best Evening Panel Award, 1986 International Solid-State Circuits Conference (as panel member)

Beatrice Winner Editorial Excellence Award, 1987 International Solid-State Circuits Conference (co-recipient)

1987 Circuits and Systems Society Technical Achievement Award (co-recipient)

Best Paper Award, IEEE Solid-State Circuits Journal, 1991 (co-recipient)

Elected to National Academy of Engineering, 1990

Appointed the Edgar L. and Harold H. Buttner Professor of Electrical Engineering (Endowed Chair), 1991

IEEE Solid-State Circuits Award, 1994

Best student paper Award, 1997 International Solid-State Circuits Conference (co-recipient)

Appointed to the Roy W. Carlson Chair in Engineering, (Endowed Chair), 1996

Honorary Doctorate, University of Bucharest, Romania, October 1999

IEEE Third Millennium Medal, IEEE Solid-State Circuits Society, January 2000

CASS Golden Jubilee Medal, IEEE Circuits and Systems Society, January 2000

Appointed to the Andrew Grove Distinguished Professorship in Engineering, 2000

National Outstanding Researcher Award, Semiconductor Industry Association, Spring 2000

Outstanding Paper Award, 2001 IEEE International Solid-State Circuits Conference, February 2002
(co-recipient)

2004 IEEE James H. Mulligan, Jr. Education Medal

2005 American Society for Engineering Education Benjamin Garver Lamme Award

Best student paper award, 2004 IEEE International Solid-State Circuits Conference (co-recipient)

Honorary Doctorate, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, 2006

2008 IEEE Robert Noyce Medal

Publications

Books

1. P.R. Gray, P. Hurst, S. Lewis, R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", 4th Edition, January 2001

Papers

1. "Large Signal and Small Signal Models for Arbitrarily Doped Four-Terminal Field-Effect Transistors," (with F. A. Lindholm) *IEEE Transactions on Electron Devices*, Vol. ED-13, December 1966.

2. "An Automatic Polarimeter for Space Applications," (with S. F. Pellicori) *Applied Optics*, Vol. 6, June 1967.

3. "Electrothermal Integrated Circuits," (with D. J. Hamilton) presented at the International Solid State Circuits Conference, Philadelphia, PA, February 1970. Also appeared in *IEEE Journal of Solid State Electronics*, February 1971.

4. "A 15 Watt Monolithic Power Operational Amplifier," presented at the International Solid State Circuits Conference, Philadelphia, PA, February 1972. Also appeared in *IEEE Journal of Solid State Circuits*, December 1972.

5. "Electro-Thermal Interactions in Integrated Circuit Design," International Symposium on Circuit Theory, Toronto, Ontario, Canada, April 1973.

6. "A Fast-Settling Monolithic Operational Amplifier Using Doublet Compression Techniques," (with R. J. Apfel) *Digest of Technical Papers*, 1974 International Solid State Circuits Conference, February 1974. Also in *IEEE Journal of Solid State Circuits*, December 1974.

7. "A Completely Monolithic Sample-Hold Amplifier Using Compatible Bipolar and Silicon Gate FET Devices," (with K. Stafford and R. Blanchard) *Digest of Technical Papers, 1974 International Solid State Circuits Conference*, February 1974. Also in *IEEE Journal of Solid State Circuits*, December 1974.

8. "An All-MOS Charge-Redistribution A/D Converter Using Charge Redistribution Techniques," (with J. McCreary and D. A. Hodges) *Digest of Technical Papers*, 1974 International Solid State Circuits Conference, February 1974.

9. "An MOS-Compatible Analog-Digital Converter Using Charge-Redistribution Techniques," (with R. Suarez-Gartner and D. A. Hodges), *Digest of Technical Papers*, 1974 International Solid State Circuits Conference, Philadelphia, PA, February 1974.

10. "Analysis and Design of Temperature Stabilized Substrate Integrated Circuits," (with D. J. Hamilton and D. J. Lieux) *IEEE Journal of Solid State Circuits*, April 1974.

11. "Recent Advances in Monolithic Operational Amplifier Design," (with R. G. Meyer) *IEEE Transactions on Circuit Theory*, April 1974.

12. "Relationship Between Frequency Response and Settling Time of Operational Amplifiers," (with B. Kamath and R. G. Meyer) *IEEE Journal of Solid State Circuits*, December 1974.
13. "A High Speed, All-MOS Successive-Approximation Weighted Capacitor A/D Conversion Technique," (with J. L. McCreary) *Digest of Technical Papers*, 1975 International Solid State Circuits Conference, Philadelphia, Pennsylvania, February 1976 (Best paper award).
14. "All-MOS Charge-Redistribution Analog-Digital Conversion Techniques, Part I," (with J. L. McCreary) *IEEE Journal of Solid State Circuits*, Vol. SC-10, No. 6, pp. 371-378, December 1975.
15. "All-MOS Charge-Redistribution Analog-Digital Conversion Techniques, Part II," (with R. E. Suarez and D. A. Hodges), *IEEE Journal of Solid State Circuits*, Vol. SC-10, No. 6, pp. 379-384, December 1975.
16. "An All-MOS Companded PCM Voice Encoder," (with J. Tsividis, D. A. Hodges and J. Chacko), *Digest of Technical Papers, 1976 International Solid State Circuits Conference*, Philadelphia, Pennsylvania, pp. 24-25, February 1976. (Also appeared in *International Solid-State Circuits Journal*, December 1976.)
17. "Non-CCD MOS Analog Circuits for Signal Processing," (with D. A. Hodges and Y. P. Tsividis), (invited paper), *Digest of Technical Papers, 19th Midwest Symposium on Circuits and Systems*, Madison, Wisconsin, pp. 427-429, August 1976.
18. "Computer Simulation of Monolithic Circuit Performance in the Presence of Electro-Thermal Interactions," (with K. Fukahori), *Digest of Technical Papers, 1976 International Solid State Circuits Conference*, Philadelphia, Pennsylvania, pp. 112-113, February 1976. *International Solid-State Circuits Journal*, December 1976.
19. "An Integrated NMOS Operational Amplifier with Internal Compensation," (with Y. P. Tsividis and D. A. Hodges), *IEEE Journal of Solid-State Circuits*, Vol. SC-11, No. 6, pp. 748-752, December 1976.
20. "A Segmented u-255 Law PCM Voice Encoder Utilizing NMOS Technology," (with Y. P. Tsividis, D. A. Hodges, and J. Chacko), *IEEE Journal of Solid State Circuits*, Vol. SC-11, No. 6, pp. 740-747, December 1976.
21. "Analog NMOS Sampled-Data Recursive Filter," (with I. A. Young and D. A. Hodges), *Digest of Technical Papers, 1977 International Solid State Circuits Conference*, Philadelphia, PA, pp. 156-157, February 1977.
22. "Computational Considerations in the Simulation of Monolithic Integrated Circuits with Electro Thermal Interactions," (with K. Fukahori), *Digest of Technical Papers, 1977 International Symposium on Circuits and Systems*, Phoenix, Arizona, pp. 68-69, April 1977.
23. "MOS Sampled-Data Recursive Filters Using State Variable Techniques," (with B. J. Hosticka and R. W. Brodersen), *Digest of Technical Papers, 1977 International Symposium on Circuits and Systems*, Phoenix, Arizona, pp. 525-526, April 1977 (Invited).
24. "Potential of MOS Technologies for Analog Integrated Circuits," (with D. A. Hodges and R. W. Brodersen), *Digest of Technical Papers, European International Solid State Circuits Conference*, Ulm, Germany, September 1977. Invited paper (best paper).
25. "MOS Sampled-Data Recursive Filters Using Switched Capacitor Integrators," (with B. J. Hosticka and R. W. Brodersen), *IEEE J. of Solid State Circuits*, pp. 600-609, December 1977.
26. "A High Voltage Analog-Compatible $1\mu\text{m}$ Process," (with D. J. Allstot, T. S. Wei, S. K. Lui, and R. G. Meyer), *Digest of Technical Papers, 1977 International Electron Devices Meeting*, Washington, D.C., December 1977.

27. "Analysis and Design of Analog Integrated Circuits," (with R. G. Meyer), Wiley & Sons, 1977.
28. "Computer Simulation of Integrated Circuits in the Presence of Electrothermal Interactions," (with K. Fukahori), *IEEE Journal of Solid-State Circuits*, SC-11, No. 6, pp. 834-837, December 1977.
29. "MOS Sampled-Data Recursive Filters Using State Variable Techniques," (with B. J. Hosticka and R. W. Brodersen), *IEEE Journal of Solid State Circuits*, pp. 600-609, December 1977.
30. "High-Order Monolithic Analog Filters Using Bipolar/JFET Technology," (with K. S. Tan), *Digest of Technical Papers, 1978 International Solid State Circuits Conference*, San Francisco, CA, February 1978.
31. "Fully-Integrated High-Order NMOS Sampled-Data Ladder Filters," (with D. J. Allstot and R. W. Brodersen), *Digest of Technical Papers, 1978 International Solid State Circuits Conference*, San Francisco, CA, February 1978.
32. "All-MOS Analog-Digital Conversion Techniques – An Overview," (with D. A. Hodges), *Digest of Technical Papers, International Symposium on Circuits and Systems*, New York, May 1978 (invited paper).
33. "Design Considerations for Switched-Capacitor Ladder Filters," (with G. J. Jacobs, D. J. Allstot, and R. W. Brodersen), *Digest of Technical Papers, International Symposium on Circuits and Systems*, New York, May 1978.
34. "Potential of MOS Technologies for Analog Integrated Circuits," (with D. A. Hodges and R. W. Brodersen), *IEEE J. of Solid State Circuits*, pp. 285-294, June 1978.
35. "A New High-Voltage Analog-Compatible $1\mu\text{m}$ Process," (with D. J. Allstot, S. K. Lui, T. S. T. Wei and R. G. Meyer), *IEEE Journal of Solid State Circuits*, Vol. SC-13, No. 4, August, 1978.
36. "Switched-Capacitor Filters for Telecommunications Applications," (with R. W. Brodersen, D. A. Hodges, D. J. Allstot, and G. Jacobs), *Digest of Technical Papers, 1978 European Conference on Circuit Theory and Design*, Lausanne, Switzerland, September 1978.
37. "CMOS Pulse Code Modulation Codec," (with G. Smarandoiu, D. A. Hodges, and G. F. Landsburg), *IEEE Journal of Solid State Circuits*, Vol. SC-113, No. 4, pp. 504-510, August 1978.
38. "Considerations for the Implementation of Switched Capacitor Filters," (with D. J. Allstot and R. W. Brodersen), *1978 Asilomar Conference on Circuits and Systems*, Asilomar, California, November 1978.
39. "High Performance NMOS Operational Amplifier," (with D. Senderowicz and D. A. Hodges), *IEEE Journal of Solid State Circuits*, Vol. SC-213, No. 6, pp. 760-767, December 1978.
40. "NMOS Switched Capacitor Ladder Filters," (with D. J. Allstot and R. W. Brodersen), *IEEE Journal of Solid State Circuits*, Vol. SC-13, No. 6, pp. 806-814, December 1978.
41. "Fully Integrated Analog Filters Using Bipolar-JFET Technology," (with K. S. Tan), *IEEE Journal of Solid State Circuits*, Vol. SC-13, No. 6, December 1978.
42. "Design Techniques for MOS Switched Capacitor Ladder Filters," (with D. J. Allstot, G. M. Jacobs, and R. W. Brodersen), *IEEE Trans. on Circuits and Systems*, Vol. CAS-25, December 1978.
43. "MOS Switched Capacitor Filters, An Overview," (with R. W. Brodersen and D. A. Hodges),

Digest of Papers, 1979 *International Symposium on Circuits and Systems*, Tokyo, Japan, July 1979 (Invited paper).

44. "A Single Chip NMOS Dual Channel Filter for PCM Telephony Applications," (with D. Senderowicz, H. Ohara, and B. W. Warren, *IEEE Journal of Solid State Circuits*, Vol. SC-14, No. 6, pp. 981-991, December 1979.

45. "Electrically-Programmable Switched-Capacitor Filter," (with D. J. Allstot and R. W. Brodersen), *ibid*, pp. 1034-1040.

46. "A New Second-Generation Low-Power NMOS Switched-Capacitor Channel Filter," (with H. Ohara, C. Rahim, W. Baxter, and J. McCreary), *Digest of Technical Papers, International Conference on Communications*, Seattle, Washington, June 8-12, 1980. Also appeared at *IEEE Journal Solid-State Circuits*, December 1978.

47a. "Integrated Circuits for Telephony," (with D. G. Messerschmitt) *Proc IEEE*, Vol 68, no 8, Aug. 1980, pp 991-1009.

47. "Low-Noise Chopper Stabilized Differential Switched Capacitor Filtering Technique," (with K. C. Hsieh), *Digest of Technical Papers, 1981 International Solid-State Circuits Conference*, New York, NY, February 1981.

48. "Some Practical Aspects of Switched Capacitor Filter Design," (with R. W. Brodersen, D. A. Hodges, T. Choi, R. Kaneshiro, and K. C. Hsieh), *Proceedings of the 1981 IEEE International Symposium on Circuits and Systems*, Chicago, IL, April 1981.

49. "An NMOS Vector-Locked Loop," (with D. Senderowicz and D. A. Hodges), *Digest of Technical Papers, European Solid-State Circuits Conference*, September 1981.

50. "MOS Operational Amplifier Design (emA Tutorial Overview)," (invited) (with R. G. Meyer), *IEEE Journal of Solid State Circuits*, Vol. SC-17, No. 12, December 1982.

51. "An MOS Switched-Capacitor Instrumentation Amplifier," (with R. Yen), *ibid*.

52. "A Precision Curvature-Compensated CMOS Bandgap Reference," (with B. S. Song), *Digest of Technical Papers, International Solid-State Circuits Conference*, New York, February 1983.

53. "High-Frequency CMOS Switched Capacitor Filters for Communications Applications," (with T. C. Choi, R. T. Kaneshiro, R. W. Brodersen, B. Jett, and M. Wilcox), *ibid*.

54. "High-Frequency Switched Capacitor Filtering Techniques," (with R. T. Kaneshiro, T. C. Choi, and R. W. Brodersen), *Digest of Papers, 1983 International Symposium on Circuits and Systems*, Newport Beach, CA, May 1983.

55. "Integrated Circuits for Local Digital Switching Line Interfaces," (with D. G. Messerschmitt), *Tutorials in Modern Communications*, Computer Sciences Press, Rockville, Maryland, 1983.

56. "The Role of Analog Circuits in VLSI Technologies of the Future," (with R. W. Brodersen), *Digest of Papers, 1983 European Solid-State Circuits Conference*, Lausanne, Switzerland, September 1983.

57. "A Precision Curvature-Corrected CMOS Bandgap Reference," (with B. S. Song), *IEEE Journal of Solid-State Circuits*, Vol. SC-18, No. 6, December 1983.

58. "High-Frequency CMOS Switched-Capacitor Filters for Telecommunications Applications," (with T. C. Choi, R. T. Kaneshiro, R. W. Brodersen, W. B. Jett, and M. Wilcox), *IEEE Journal of Solid-State Circuits*, Vol. SC-18, No. 6, December 1983.

59. "A Ratio-Independent Algorithmic A/D Conversion Technique," (with P. W. Li and R. Castello), *Digest of Technical Papers, 1984 International Solid-State Circuits Conference*, February 1984.
60. "A Self-Calibrating 12 bit, 12 μ s CMOS ADC," (with H. S. Lee and D. A. Hodges), *Digest of Technical Papers, 1984 International Solid-State Circuits Conference*, February 1984.
61. "A Programmable CMOS Dual-Channel Interface Processor," (with B. K. Ahuja and W. M. Baxter), *Digest of Technical Papers, 1984 International Solid-State Circuits Conference*, February 1984.
62. "Performance Limits in VLSI Data Converters," (with D. A. Hodges), *Digest of Technical Papers, 1984 IEEE International Symposium on Circuits and Systems*, Montreal, Canada, May 1984.
63. "High-Frequency CMOS Continuous Time Filtering Techniques," (with H. Khorramabadi), *Digest of Papers, 1984 IEEE International Symposium on Circuits and Systems*, Montreal, Canada, May 1984.
64. "High-Frequency CMOS Continuous-time Filters," (with H. Khorramabadi), *IEEE Journal of Solid State Circuits*, Vol SC-19, no 6, December, 1984, pp 932-938.
65. "A Programmable CMOS Dual Channel Interface Processor for Telecommunications Applications," (with B. Ahuja and W. Baxter), *IEEE Journal of Solid-State Circuits*, Vol SC-29, No 6, December, 1984.
66. "A Self-Calibrating 15-bit CMOS A/D Converter," (with H. Lee and D. A. Hodges), *IEEE Journal of Solid-State Circuits*, Vols SC-19, no 6, December, 1984, pp 813-819 NSF21390, Micro.
67. "A Ratio-Independent Algorithmic A/D Converter," (with P. Li, M. Chin) Castello), *IEEE Journal of Solid-State Circuits*, Vol SC-19, no 6, December, 1984, pp 828-836.
68. "Performance Limitations in Switched Capacitor Filters," (with R. Castello), *Proceedings of the International Symposium on Circuits and Systems*, Kyoto, Japan, May, 1985, pp 247-250.
69. "A 350 Microwatt Fifth-Order Lowpass Switched Capacitor Filter," (with R. Castello) *Digest of Technical Papers, 1985 International Solid-State Circuits Conference*, New York, N. Y., February, 1985, pp 276-278.
70. "Analog-Digital Conversion Techniques for Telecommunications Applications," (with D. A. Hodges), Book Chapter, *Design of MOS/VLSI Circuits for Telecommunications*, Prentice-Hall, 1985.
71. "Performance Limitations in Switched Capacitor Filters," (with R. Castello), Book Chapter, *Design of MOS/VLSI Circuits for Telecommunications Applications*, Prentice-Hall, 1985.
72. "A High Performance Micropower Switched Capacitor Filter," (with R. Castello) *IEEE Journal of Solid State Circuits*, Vol SC-20, No 6, December, 1985.
73. "Performance Limitations in Switched Capacitor Filters," (with R. Castello), *IEEE Transactions on Circuits and Systems*, Vol CAS 32, No 9 October, 1985.
74. "Reference-Recirculation Algorithmic A/D Conversion Techniques," (with C. Shih), *Digest of Technical Papers 1986 International Symposium on Circuits and Systems*, Santa Clara, May, 1986.
75. "A Scalable High-Performance Switched-Capacitor Filter," (with C.K. Wang and R. Castello), *Digest of Technical Papers, 1986 International Symposium on Circuits and Systems*, Santa Clara, May, 1986.
76. "A Scalable High-Performance Switched Switched-Capacitor Filter," (with C. K. Wang and R. Castello), Joint Special Issue on Integrated Circuits for Signal Processing, *IEEE Journal of Solid State Circuits and IEEE Transactions on Circuits and Systems*, February, 1986.

77. "A High-Performance 3 micron Analog Standard Cell Library," (with C. Rahim, G. Uehara, P. Kwok, S. Dreyer), *Digest of Technical Papers, 1986 IEEE Custom Integrated Circuits Conference*, Rochester, New York, May, 1986.
78. "Reference Refreshing Cyclic Analog to Digital and Digital to Analog Converters," (with C. Shih) *IEEE Journal of Solid State Circuits*, Vol SC-21, no 4, August, 1986.
79. "High-Frequency CMOS Switched Capacitor Filters," (with B. S. Song) *IEEE Journal of Solid State Circuits*, Vol SC-21, no 6, December 1986.
80. "Recent Developments in A/D Interfaces for Signal Processing," (with R. W. Brodersen), *VLSI Signal Processing II*, IEEE Press, November, 1986.
81. "Automatic Compilation of Switched Capacitor Filters," (with P. Hormuz and A. Sangiovanni-Vincentelli), *Digest of Technical Papers, 1986 International Conference*.
- 82 "Design Considerations for a High-Performance 3u CMOS Analog Standard Cell Library," C. A. Laber, C. F. Rahim, S. Dreyer, G. Uehara, P. Kwok. R. Gray, *IEEE Journal of Solid-State Circuits*, April, 1987.
- 83 "A CMOS Programmable Self-Calibrating 13-bit Eight-Channel Analog Interface Processor," M. Armstrong, H. Ohara, H. Ngho, and P. R. Gray, *Digest of Technical Papers, 1987 IEEE International Solid-State Circuits Conference*, New York, N. Y., February, 1987.
84. "A Pipelined 5mhz 9bit ADC," S. Lewis and P. R. Gray, *Digest of Technical Papers, 1987 IEEE International Solid-State Circuits Conference*, New York, N. Y., February, 1987.
85. S. Lewis and P. R. Gray, "A 9-bit 5 Mhz Pipelined Analog-Digital Converter," *IEEE Journal of Solid-State Circuits*, December, 1987.
86. H. Ohara, H. Ngho, M. Armstrong, C. Rahim, and P. R. Gray, "A CMOS Programmable Self-Calibrating 13-bit 8-channel Data Acquisition Peripheral," *IEEE Journal of Solid-State Circuits*, December, 1987.
- 87 H. Koh, C. Sequin, and P. R. Gray, "Automatic Synthesis of Operational Amplifiers Based on Analytic Circuit Models," *Digest of Technical Papers, IEEE ICCAD*, November, 1987.
88. P. R. Gray, "Analog ICs in the Submicron Era: Trends and Perspectives," Invited Plenary Paper, 1987 International Electron Devices Meeting, Washington, DC, December, 1987.
89. S. Sutardja and P. R. Gray, "A 250ks/sec, 13b 5V 15mW Pipelined ADC in a 3u CMOS Process," *Digest of Technical Papers, 1988 IEEE International Solid-State Circuits Conference*, February, 1988.
90. B. Leung, R. Neff, P. R. Gray, and R. W. Brodersen, "A Four-Channel Oversampled CMOS PCM Voiceband Coder," *Digest of Technical Papers, 1988 IEEE Solid-State Circuits Conference*, February, 1988.
91. H. Yaghutiel, S. Shen, A. Sangiovanni Vincentelli, and P. R. Gray, "Automatic Layout of Switched-Capacitor Filters," *Digest of Technical Papers, 1988 International Solid-State Circuits Conference*, San Francisco, CA, February 1988.
- 92 J. Doernberg, D. A. Hodges, P. R. Gray, "A 10Mbit, 5Msample/sec CMOS 2-step Flash ADC, *IEEE Journal of Solid-State Circuits*," Vol SC-24, No 1, February 1989.
93. S. Sutardja and P. R. Gray, "A 13b 5V 15mW Pipelined Analog-Digital Converter Using Reference Feedforward Techniques," *IEEE Journal of Solid-State Circuits*, Vol SC-23, No 6, December, 1988.

94. B. Leung, R. Neff, P. R. Gray, and R. W. Brodersen, "Area Efficient Multi-Channel Oversampled PCM Voiceband Coder," *IEEE Journal of Solid-State Circuits*, Vol SC-23, no 6, December, 1988.
95. C. Laber and P. R. Gray, "Broadband, High-Q Switched Capacitor Filters Using Internal Positive Feedback," *IEEE Journal of Solid-State Circuits*, Vol SC-24, no 6, December, 1988.
96. P. R. Gray, B. Wooley, and R. W. Brodersen, editors, "MOS Analog Integrated Circuits, Second Edition," IEEE Reprint Volume, January 1989.
97. H. Koh, C. Sequin, and P. R. Gray, "Automatic Layout Generation for CMOS Operational Amplifiers," *Digest of Technical Papers, ICCAD-88*, November, 1988, Santa Clara, CA.
98. S. Shieh, C. K. Wang, R. Castello, and P. R. Gray, "A Scalable Switched Capacitor Filter Implemented in 1.5 Micron Technology," (Correspondence Item) *IEEE Journal of Solid-State Circuits*, vol SC-24, no 1, February, 1989.
99. H. Koh, C. Sequin, and P. R. Gray, "Automatic Layout Generation for CMOS Operational Amplifiers," *Digest of Technical Papers, ICCAD-88*, November, 1988, Santa Clara, CA.
100. E. S. Kim, R. S. Muller, and P. R. Gray, "Integrated Microphone with CMOS Circuits on a Single Chip," *Digest of Papers, 1989 International Electron Devices Meeting*, Washington, December, 1989.
101. B. Kim, D. Helman, P. R. Gray, "A 30Mhz, High-Speed Analog/Digital PLL in 2 Micron CMOS," *Digest of Papers, 1990 International Solid-State Circuits Conference*, San Francisco, February, 1990.
102. H. Y. Koh, C. H. Sequin, and P. R. Gray, "OPASYN, A Compiler for CMOS Operational Amplifiers," *IEEE Trans on CAD*, Vol 9, No 2, February, 1990, pp 113-125.
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