

EE240 Design Project: A Fiber-optic Wideband Transimpedance Pre-amplifier

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Introduction

The end-goal of this project was to design a monolithic, fiber-optic preamplifier that created an input current to output voltage amplification of 20 kΩ. Through a long and arduous process of hand design and then SPICE simulation, the end result (see Fig. 1 on the next page) is a circuit that meets most of the specifications, but unfortunately does not meet them all. It also runs into problems over process variation. Try as I might, I could not get the basic topology I was using to be insensitive to those variations.

The basic design process I went through is explained in the Design Process section. After that, section, in the Summary of Results section, I have tabulated my results, along with attempts to explain some of the problems and reasons why certain specifications were not met. Finally, following that section, are the hand calculations and SPICE results.

Design Process

This project specified a current-in, differential

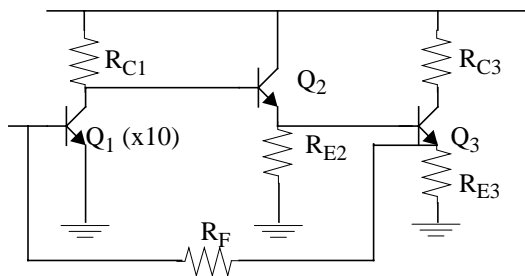


Fig 2. Current Feedback pair with Darlington Output voltage-out circuit, so one possible topology for the input was to use a current-feedback pair with

Darlington output (CFBP - Fig. 1.) to amplify the current, and then have a second stage of voltage amplification to meet the overall gain specification. This stage was the most important one for noise, as the noise beyond this stage would be reduced by the gain of the CFBP when being converted to equivalent input noise, so my first concern was to try to keep the noise down as much as possible. The equivalent input noise of the CFBP is defined by the following equation:

$$\overline{i_{eq}^2} = 4kT \frac{1}{R_F} \Delta f + 2qI_{B1} \Delta f + 2qI_{C1} \frac{1}{g_{m1}^2} \omega^2 (C_s + C_{\pi1})^2 \Delta f + 4kTr_{b1} \omega^2 C_s^2 \Delta f$$

I originally started by trying to make the noise less than about 35nA for the input stage. At that time, I thought that the gain of the input stage would effectively prevent noise from later stages from having an effect at the input. It is clear from the equation that in order to decrease the noise, one needs to:

1. Make R_F as large as possible.
2. Make the bias current I_{C1} (and therefore I_{B1}) as small as possible.
3. Make $C_{\pi1}$ as small as possible.
4. Make r_{b1} as small as possible.

However, these values cannot be made indiscriminately large or small: they control many other factors of operation in this circuit, and therefore, one has to be careful that other specifications are not compromised.

I therefore went through some hand calculations to find out what values of R_F would satisfy the

35nA noise I limit I had set for myself for different values of I_{C1} , and found that for a minimum size input transistor, my R_F would be prohibitively large (on the order of 30k Ω)! I realized immediately that a feedback resistor this size would cause problems for both the distortion and bandwidth specifications, and therefore I realized that I would have to change the other parameters as well. To that end, I started increasing the size of the input transistor, which would increase $C_{\pi1}$, but would also decrease r_{b1} . Since $C_{\pi1}$ was swamped by C_s for worst case noise, the effect of reducing r_{b1} outweighed the increase in $C_{\pi1}$. Accordingly, the requirement on R_F reduced to about 6-7 k Ω for I_{C1} in the 0.3 to 0.4 range for a x10 input npn transistor.

The other specification that put a stringent requirement on R_F was the input overload current point. This point is limited by the following two equations:

$$I_{oc}R_F < V_{BE1}$$

$$I_{C3} > I_{OC} \times \left(1 + \frac{R_F}{R_{E3}}\right), \text{ where } (1 + R_F/R_{E3}) \text{ is the}$$

current gain of the CFBP. Thus in this case, for R_F in the range 6k Ω to 7k Ω and I_{C1} of about 250 μ A, we find that the input overload current point is over 100 μ A, which for this project is just fine. I decided to make R_F 6k Ω , as a higher R_F hurts the bandwidth of the circuit, and causes the input overload current to be closer to the low end of the hand-calculated input overload current point, and leaving as much leeway as possible is always helpful.

The bandwidth of the CFBP is determined by the input transistor. We see that the C_u of the first stage is increased by the Miller effect; the second stage is an emitter-follower, which has excellent frequency response, and the final transistor is emitter-degenerated, and so has much smaller gain. Thus the dominant pole of this stage comes at the input. Likewise, the second pole comes from the collector of first transistor, as it is a high impedance node with the largest intrinsic capacitances of this stage (the input transistor is x10). Therefore, the

frequency response of the CFBP stage can be determined using the following approximate circuit:

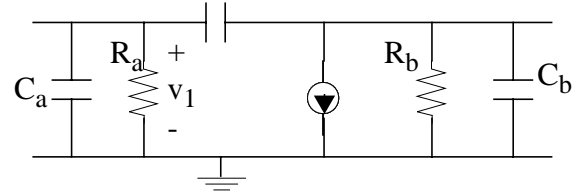


Fig 3. Equivalent Ckt. For Freq. Resp. Calc.

The dominant pole of this system is given by

$$p_1 = -\frac{1}{(C_b + C_{\mu1})R_b + (C_a + C_{\mu1})R_a + g_{m1}R_aR_bC_{\mu1}}$$

The second pole is given by

$$p_2 = -\frac{g_{m1}C_{\mu1}}{C_aC_b + C_{\mu1}(C_a + C_b)}$$

The second pole will dominate the frequency response once the circuit is put into feedback. The second pole controls the location where the two poles will meet (according to Root-Locus rule #6) at approximately 1/2 the value of the non-dominant pole for a two-pole system. So in order to get 250 MHz, bandwidth, the second pole must be greater than 500 MHz. For the numbers mentioned above, we find that the second pole is situated at 677 MHz. Thus this selection of R_F and I_{C1} satisfies the bandwidth specification as well.

The transimpedance of the first stage is approximately given by

$$R_{CFBP} = R_F \frac{R_{C3}}{R_{E3}}$$

I wanted to ensure that I didn't need large resistors in my second stage (so I could avoid high impedance nodes and assume that the above frequency analysis applied for the most part to the entire circuit), so I wanted to get a good amount of gain out of this first stage. With the above value of

R_F (6 k Ω), we see that even with the collector and emitter resistors being the same, we can still get $V_O/I_i=6000$. This leaves me with only a gain requirement of between 3 and 4 in the next stage, which did not seem that difficult to meet.

Second Stage: Differential Pair

From the current feedback pair, the signal had to be converted to a differential voltage signal. The easiest way to do this is to apply the output of the CFBP to one side of a differential pair (DP), and tie the other side to AC ground (with some sort of DC biasing so that the two sides will be matched).

The requirements on the signal at the output of this stage included a maximum of 50mV output offset, output swing of (at least) 1.8 V, and a small signal gain of at least 20k Ω .

I originally tried to tie the output of the CFBP directly to the input of one side of the DP, and biased the other side by trying to match the number of diode drops and resistor drops between V_{CC} and the input of the DP. Assuming no DC voltage drop across R_F , R_{E3} has the V_{BE} of Q_1 across it. I originally had $R_{E3}=R_{C3}$, so R_{C3} also had one V_{BE} drop across it, and thus the collector of Q_3 was at one V_{BE} below V_{CC} . This seemed very easy to match on the bias side of the DP - a single diode would match the two sides.

However, at this stage, problem after problem arose. I ran into problems with both the DP transistors saturating and the I_{EE} current source transistor saturating. In order to avoid the DP transistors saturating, I needed to bring the DC bias point at the input of the DP down, but in order to avoid saturating the I_{EE} transistor, I had to bring the bias point up. Eventually, after many trials, I found that the best bias point I could obtain came from (1) making $R_{C3}=2R_{E3}$ (to increase the drop across R_{C3} to $2V_{BE}$), and (2) to increase the ratio of the resistive divider resistors to about 1:2 (to lose some of the gain out of the CFBP - otherwise the input node of the DP swings too much). This does bring the bias point somewhat low, but by make the

emitter resistor of the current source very small (50 Ω), the headroom there is increased enough to keep the DP operational.

Once that was determined, however, matching between both sides became a serious problem. I tried to match the two sides of the circuit by matching diode drops and resistor drops, but that method was too sensitive to both temperature variation and power supply variation (my Power Supply Rejection Ratio (PSRR) was on the order of -26 dB). It seemed like I could play around with that matching scheme (similar to the one used in the transimpedance amp. by Meyer and Blauschild) to get the output offset down to zero at one temperature and power supply, but not over the variation in the two. Therefore, I decided to duplicate the CFBP on the other side of the DP. This gives perfect matching over temperature, power supply, and process variation. There is decidedly a power increase as well as a noise increase, but the PSRR is reduced dramatically. The noise from the non-input side of the DP can be reduced by using a capacitor to ground at the base of the DP transistor on that side, effectively creating a low-pass filter and preventing any high-frequency noise from that side of the DP from going through to the output.

The gain through the DP is determined by the ratio of the collector to emitter resistors in the DP. Since I needed a gain of just over four through the DP (I had a gain of about 6k coming out of the CFBP and the resistive divider), I chose to use 1500 Ω as the collector resistor, and 400 Ω as the emitter resistor. The values may seem a little large, but the larger the resistor, the lower the current needs to be to give a 1.8 V swing at the output, and thus power consumption can be decreased.

That brings us to the current source. Another problem arose because the simple resistor based current source is too sensitive to power supply variations, and thus at worst-case rails, my current dropped too much, and my output was not able to swing the (minimum) 1.8 V needed to meet the

input overload current spec. Therefore, I went to a V_{BE} -reference current source. In the simplest case, this current source is logarithmically proportional to current, and thus the current stays much closer to its nominal value than it would in the simple current source.

Finally, we come to the output rise and fall time matching specification. This was easily the hardest specification to meet at nominal. Try as I might, I just couldn't get the rise and fall times to match closely. One explanation about the transient analysis: from talking to several people, it seemed clear that if the circuit was run with a large, repeating input pulse, the average DC value of the output would be at the middle of the swing. This value is the output for the average DC input value. In this case, since the maximum pulse size is 90 μA , we can say that the average DC input value is 45 μA . To simulate what happens to the output after a large number of cycles, we can start the input pulse off at 45 μA , and then swing between 0 and 90 μA . This sets the average DC output value at 0V, and thus the swing is (minimum) $\pm 0.9\text{ V}$ around 0. This is the case I simulated. Unfortunately, I was unable to make the rise and fall times match to the properly. I was able to meet the 5% mismatch at certain extreme temperatures and supply values, but not at nominal. I tried running more current through the output buffers, but that just decreased both rise and fall times, and the difference stayed about the same. Not only that, but the increase in power was dramatic. Therefore, I decided to let that specification go.

Conclusion

This project was decidedly a very challenging one, much as it was described as from the first day of class. However, even though I was unable to meet all the specifications listed in the project handout, I did learn a great deal about analog design. Just doing the project and listening to what everyone else was doing, listening to their problems, and encountering a world of problems on my own helped me understand a great deal more about analog design than I thought I ever would. This was

decidedly a great design project. Unfortunately, I did not have the time I would have liked to put in to the project, as other outside factors (namely other classes) ended up taking a great deal of my time over the course of the semester, and so my design may not be as creative as other designs. However, this is still a good design, and with more time, it probably could have met most if not all the specs.