Noise Models for MOSFETs in Saturation

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Abstract - **Progress in CMOS device technology has motivated the design of high-performance analog integrated circuits in standard CMOS processes. In particular, the high speed of submicron CMOS devices make them attractive for a variety of analog applications, including data converters, switched capacitor circuits, and low noise amplifiers [1,2,16]. However, recent reports have indicated that the measured noise in short-channel MOSFET devices is greater than the amount predicted by long-channel theory [3,4,5]. In order to predict the noise performance of analog circuits designed using short-channel MOSFET devices, an accurate noise model is imperative. In this work, a MOSFET noise model is presented which matches well with observed data. This model accounts for the effect of high fields on the thermal noise of the device as well as the effect of substrate shot noise on the total noise current.**

I. Introduction

This work begins with an examination of the traditional noise model and its shortcomings. Since the MOSFET channel material is resistive, it exhibits thermal noise. In analog circuits, most devices are operating in the saturation region, and according to long-channel theory, the drain current noise spectral density in saturation may be expressed as

$$S_{I_d}(f) = 4kT\frac{2}{3}g_m, \qquad (1)$$

where g_m is the transconductance [6]. Eq. 1 assumes that the device is operating at frequencies well above the flicker noise corner frequency so that flicker noise may be neglected. This model underestimates the actual noise present in short-channel devices by a factor ranging from three to ten times [3,4,5].

A more accurate noise model must account for high-field effects. While these effects are also known as short-channel effects, they are present in all devices and can degrade performance at high terminal voltages. As such, an accurate noise model for any device must account for these effects which can degrade performance in the following ways. First, at high electric fields, the carrier velocity saturates, resulting in a corresponding decrease in effective mobility [7]. Second, the effective channel length decreases as V_d is increased beyond V_{dsat} due to the velocity saturation region which has length ΔL [7]. Although channel length modulation (CLM) is also present in long-channel devices, ΔL may be a significant portion of the overall channel length in short-channel devices. Third, the threshold voltage decreases with decreasing channel length and with increasing drain bias due to drain-induced barrier lowering (DIBL) [8]. All of these effects influence the channel conductance, which is the source of the thermal noise.

Recent work has addressed these issues [9,11]; however, the result is incomplete since the noise model is derived using an equation which does not hold for short-channel devices. Furthermore, hot electrons exist when high electric fields in MOSFET devices cause electrons to have a carrier temperature (T_e) which varies with the electric field and exceeds the lattice temperature (T). This alone increases the amount of thermal noise in the device[12]. Moreover, these hot electrons may cause impact ionization resulting in electron-hole pair generation; the generated electrons are collected by the drain, and the holes give rise to substrate current. The substrate current exhibits shot noise since this current is due to carriers crossing a potential barrier at random. It has been found that the measured noise due to impact ionization is greater than this shot noise [10]. Models to account for this enhancement have been proposed [10,11]; in this work, a new model based on a different interpretation of this enhancement is presented.

This paper presents an improved model for MOSFETs in saturation. The next section presents a derivation of the improved model which includes mobility degradation, CLM, DIBL, electron temperature, and substrate current. Section III compares simulated results with measured values and Section IV concludes this paper with some closing comments.

II. Analysis

In this section, models for the noise of MOSFETs in saturation are derived. The first of these is derived without

accounting for the deviation of electron temperature from the lattice temperature. The second model includes the effect of electron temperature on the noise. Finally, a preliminary model to account for the increase in noise at high drain voltages is discussed.

A. Noise Model without Electron Temperature

The thermal noise spectral density of a MOSFET device in any region of operation is given by

$$S_{I_d}(f) = \frac{4kT}{L^2 I_d}\int_0^{V_d} g^2(V)dV, \tag{2}$$

where $g(V)$ is the channel conductance at a given point along the channel and V is the corresponding voltage [12]. The most basic equation from which $g(V)$ can be derived is

$$I_d = g(V)\frac{dV}{dy}. \tag{3}$$

Including the effects of mobility degradation, the channel current is given by

$$I_d = \mu_{eff} W C_{OX}(V_g - V_t - V)\frac{E(y)}{1 + \frac{E(y)}{E_{sat}}}. \tag{4}$$

Eq. 4 can be put in the form of Eq. 3 in the following fashion:

$$I_d = \left[\mu_{eff} W C_{OX}(V_g - V_t - V) - \frac{I_d}{E_{sat}}\right]\frac{dV}{dy}. \tag{5}$$

The equation from which [9] starts neglects the second term in the above equation, and thus the result in that paper is incomplete. From Eq. 5, the noise spectral density is

$$S_{I_d}(f) = \frac{4kT\mu_{eff}C_{OX}\frac{W}{L_{eff}}(V_g - V_{t_{eff}})}{[(V_g - V_{t_{eff}}) + E_{sat}L_{eff}]^2}\left[\frac{2}{3}(E_{sat}L_{eff})^2 + (V_g - V_{t_{eff}})E_{sat}L_{eff} + \frac{1}{2}(V_g - V_{t_{eff}})^2\right]. \tag{6}$$

In order to account for the short-channel effects, the channel length used in Eq. 6 must be the L_{eff} of the device, allowing for CLM. Also, the threshold voltage used in the above equation must be the "effective" V_t of the device, taking into account DIBL. These two effects do not need to be included at an earlier point in the analysis, since the integration done to determine the noise spectral density assumes a fixed drain voltage, and the amount of both DIBL and CLM is fixed for a given drain voltage. It should also be noted that Eq. 6 predicts more noise than that obtained by simply modifying g_m in Eq. 1 to include high-field effects.

In the limit that $E_{sat}L_{eff}$ is much larger than (V_g-V_{teff}) (equivalent to assuming that the device is a long channel device), the above equation reduces to the standard long-channel noise model. However, in the limit that (V_g-V_{teff}) is much larger than $E_{sat}L_{eff}$, Eq. 6 simplifies to

$$S_{I_d}(f) = 4kT\frac{1}{2}\mu_{eff}\frac{W}{L_{eff}}C_{OX}(V_g - V_{teff}). \tag{7}$$

Eq. 7 predicts less noise than the long-channel model predicts, which indicates that there may be another factor that causes the noise to be enhanced. Hot electron effects may help account for the observed noise enhancement.

B. Noise Model with Electron Temperature

Under high channel electric fields, the temperature of electrons in the channel can rise above that of the lattice. This effect can increase the thermal noise of the device [12]. Eq. 2 can be modified to include the effect of electron temperature, and the result is

$$S_{I_d}(f) = \frac{4kT}{L^2 I_d}\int_0^{V_d}\left(\frac{T_e}{T}\right)g^2(V)dV, \tag{8}$$

where T_e is the electron temperature and T is the lattice temperature.

One of the more challenging aspects of including the effect of electron temperature in the noise model is finding a good model for the electron temperature. A prevalent model in the literature expresses the electron mobility as a function of the temperature as shown below [13, 14,15]:

$$\mu = \mu_0\left(\frac{T}{T_e}\right)^{1/2}. \tag{9}$$

Mobility can also be represented as a function of electric field [7]:

$$\mu = \frac{\mu_0}{\sqrt{1 + \left(\frac{E}{E_C}\right)^2}}. \tag{10}$$

Eq. 10 presents a slightly more complex and more accurate relationship than the piecewise function normally used. Equating the two and solving for T_e/T gives

$$\frac{T_e}{T} = 1 + \left(\frac{E}{E_C}\right)^2. \qquad (11)$$

Using this equation for T_e/T, the noise spectral density is found to be

$$S_{I_d}(f) = \frac{4kT\mu_{eff}\frac{W}{L_{eff}}C_{OX}(V_g - V_{t_{eff}})}{[(V_g - V_{t_{eff}}) + E_{sat}L_{eff}]^2}\left[\frac{2}{3}(E_{sat}L_{eff})^2 \right. \qquad (12)$$

$$\left. +2(V_g - V_{teff})E_{sat}L_{eff} + 2(V_g - V_{t_{eff}})^2\right]$$

Again, in the limit that $E_{sat}L_{eff}$ is much larger than (V_g-V_{teff}), the noise simplifies to the long-channel model. However, in the case of $E_{sat}L_{eff}$ being much less than (V_g-V_{teff}), Eq. 12 shows that the noise is three times larger than the standard long-channel model given in Eq. 1. Moreover, it should be noted that the actual g_m of the device (including high-field effects) is significantly less than in the long-channel case, and thus the noise would appear to be magnified even more than three times.

Still, as the drain voltage rises to large values, the noise observed increases above what Eq. 12 predicts. One effect not included in Eq. 12 which becomes important at high drain voltages is substrate current, which introduces shot noise into the drain current. This effect is examined in the next section.

C. Shot Noise due to Substrate Current

Finally, at high drain voltages, significant noise increases have been reported [10,11], and it is clear that there is noise associated with the substrate current that is generated by the high drain voltage, specifically shot noise. Shot noise is generated by the random process associated with a mobile carrier jumping a potential barrier, e.g., the potential barrier of a p-n junction. The shot noise associated with this substrate current is represented as

$$S_{I_{sub}}(f) = 2qI_{sub}. \qquad (13)$$

Unfortunately, this alone does not explain the increase in noise seen in the device [10,11]. A common explanation in the literature is to include some "avalanche" multiplication factor M in the S_{Isub} equation, and fit M to experimental data.

However, a more intuitive interpretation can be reached if the increase in drain current that accompanies the presence of I_{sub} is understood. As I_{sub} increases, the potential of the substrate starts to increase due to the resistive drop in the substrate (V_{sub}=I_{sub} R_{sub}, where R_{sub} is the effective substrate resistance seen by I_{sub}). This tends to forward bias the bulk-source junction, and thus reduce the threshold voltage, which accounts for a larger drain current than expected. Similarly, the change in V_{sub} will be a noisy process due to the noise associated with I_{sub}. The noise in V_{sub} may cause a noise process in the threshold voltage, which could add to the noise seen in the drain current.

Determining an equation for this extra noise is relatively straightforward. Assuming the shot noise spectral density from I_{sub} given by Eq. 13, the noise spectral density in V_{sub} is given by

$$S_{V_{sub}}(f) = R_{sub}^2 S_{I_{sub}}(f). \qquad (14)$$

This noise spectral density can be expressed as a noise spectral density in V_t (at least in a small signal sense) by multiplying by the ratio of V_t to V_{sub}, or

$$S_{V_t}(f) = R_{sub}^2\left(\frac{dV_t}{dV_{sub}}\right)^2 S_{I_{sub}}(f). \qquad (15)$$

Finally, this can be related to a noise spectral density in I_d through the ratio of I_d to V_t, which is equivalent in magnitude to g_m, and thus the final equation is

$$S_{I_{dsub}}(f) = \left(g_m R_{sub}\frac{dV_t}{dV_{sub}}\right)^2 S_{I_{sub}}(f). \qquad (16)$$

Eq. 16 can effectively be seen as an amplified version of the noise spectral density in I_{sub}. It should be noted that this noise enhancement factor is not constant, but rather a function of the bias conditions.

The total noise spectral density in I_d is given by the sum of Eq. 16 and Eq. 12,

$$S_{I_{dtot}}(f) = S_{I_d}(f) + S_{I_{dsub}}(f). \qquad (17)$$

III. Results

In this section, the model derived in this work is compared with measured data. Since devices from which noise data can be measured were not available at the time of this writing, this model is compared with data observed by others and presented in literature. The noise data used in this section are taken from [10, 11, 16].

Noise data from an NMOS device with characteristics as shown in Table 1 is plotted in Figure 1, along with the noise

predicted by the model in [11] as well as the model derived in

Table 1. NMOS Device Parameters [11]

Parameter	Value
W	25 μm
L	3 μm
t_{ox}	42.5 nm
N_a	2×10^{15}
V_{t0}	0.75 V
V_{gs}	5.5 V
V_{dsat}	3.29 V

this work. The model used in Figure 1 does not include the effect of the shot noise in I_{sub}. The model in [11] significantly underestimates the measured noise for all values of drain bias,

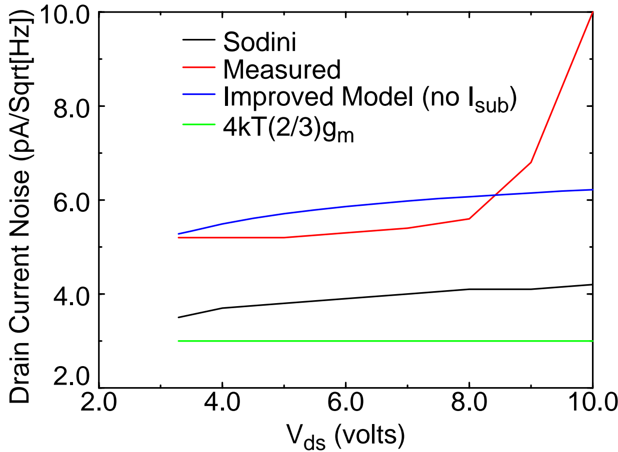

Figure 1. Drain Current Noise vs. Drain Bias for NMOS Device from [11].

deviating by as much as 29% below drain biases of 8V. However, the model presented in this work matches within nine percent for values of drain bias between 3.3 V and 8 V. Both models are inadequate at drain biases greater than 8.5 V, as the effect of noise due to substrate current becomes significant.

Figure 2 shows the improvement in the model presented in this work once the effect of substrate current noise is included. The data is again taken from a device in [11], and the observed data as well as the prediction from [11] are plotted. The model derived in this work closely matches the observed data at all values of drain bias. For this model, a value for the substrate resistance R_{sub} is required. Unfortunately, R_{sub} is a very difficult quantity to model; it is dependent on many factors, including the layout of the device, which can impact the distance to a substrate contact, and the process technology, which determines the thickness of the substrate and other factors impacting R_{sub}. For this particular case, a value of 7000 Ω was chosen as the value of R_{sub}. Since modeling R_{sub}

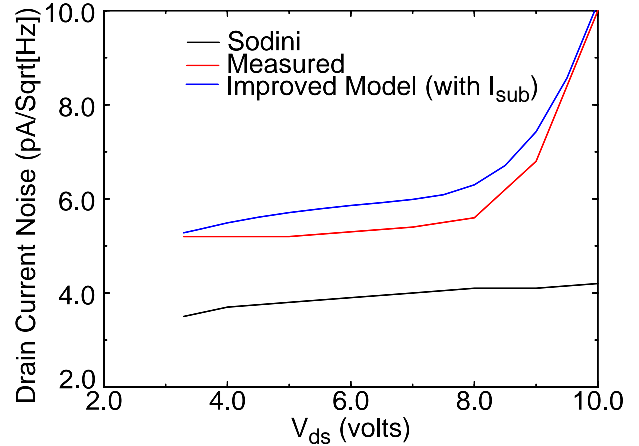

Figure 2. Drain Current Noise vs. Drain Bias for NMOS Device from [11], Including Effect of I_{sub}.

was beyond the scope of this work, a value of R_{sub} was chosen to match the drain current noise at a drain bias of 10 V.

Unfortunately, this method of determining R_{sub} may seem

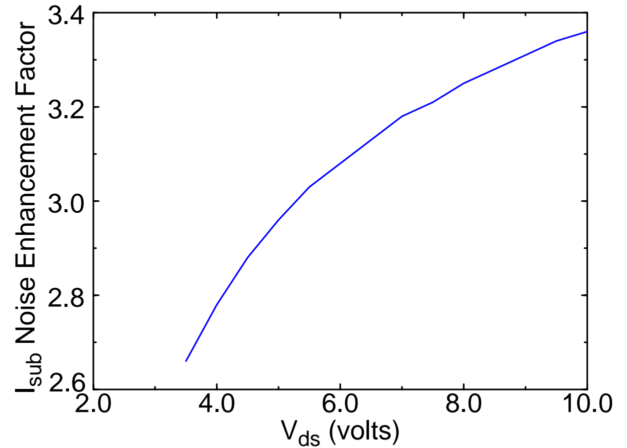

Figure 3. Effective Isub Noise Enhancement Factor for NMOS Device from [11].

similar to the method of fitting a multiplicative factor to the shot noise equation. It was stated earlier that the method of predicting the noise in this work is a more intuitive approach to explaining the noise enhancement, and yet an empirical method was still used to determine the parameter R_{sub}. However, there is one important difference between the model presented here and the other models which select an empirical multiplicative factor. It is apparent from [11] that a constant multiplicative factor M is not sufficient to account

for the noise enhancement at high drain voltages; the prediction in [11] gets less accurate with increasing V_{ds}. The method proposed in this work makes this enhancement factor a function of the terminal voltages, improving the prediction of the drain current noise. This variation in the effective multiplication factor M used in the model derived in this work is shown in Figure 3.

Figure 4 plots the predictions of drain noise current given by

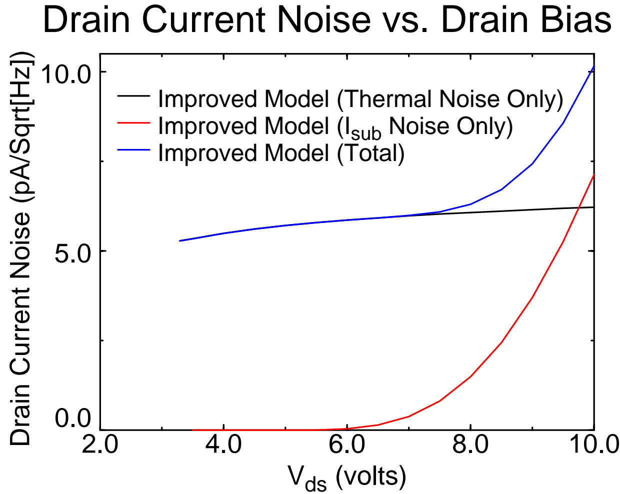

Figure 4. Comparison of Thermal Noise, I_{sub} Noise, and Total Noise Predictions from Models Derived in this Work.

Eq. 12, Eq. 16, and Eq. 17. Plotting the noise currents in this manner emphasizes the significant contribution of the noise induced by the shot noise in I_{sub} at high drain voltages.

Data for two devices was also taken from [10], whose characteristics are shown in Table 2. Figure 5 shows a comparison between the measured values of the noise enhancement factor γ (not to be confused with the body effect coefficient) and those predicted by the model presented in this work for Device A. γ is defined to be a multiplicative factor used to account for noise enhancement over the standard long-channel model, and is actually referenced to the zero-drain bias drain conductance g_{d0}, which in the long-channel model

Table 2. NMOS Device Parameters [10]

Parameter	Device A	Device B
W	1200 μm	800 μm
L	1.25 μm	.75 μm
t_{ox}	25 nm	25 nm
V_{t0}	0.53 V	0.52 V
V_{gs}	1.2 V	1.1 V
V_{dsat}	0.57 V	0.47 V

is equivalent to g_m in saturation. It is essentially a measure of the noise enhancement due to high-field effects. The model presented in this work closely matches the measured results

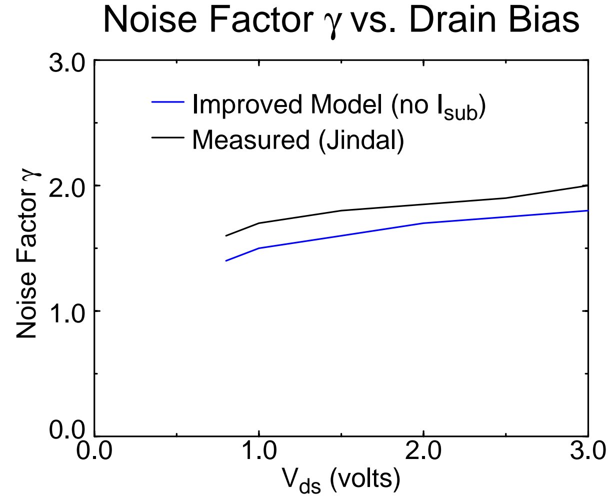

Figure 5. Noise Factor γ vs. Drain Bias for Device A from [10].

from [10]. The noise due to I_{sub} is not included in this comparison, as the drain bias is sufficiently low that I_{sub} is not yet significant.

Figure 6 shows a similar set of curves for Device B in [10].

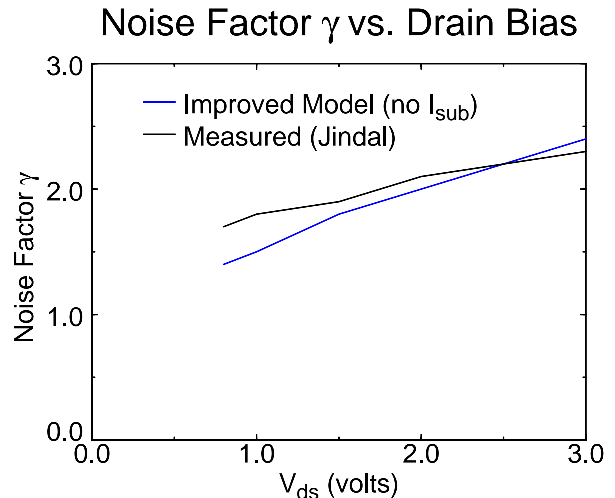

Figure 6. Noise Factor γ vs. Drain Bias for Device B from [10].

Again, the predicted and measured noise currents match closely.

Finally, the noise model was used to generate an equivalent noise figure for a 1.9 GHz low noise amplifier (LNA) designed in a 0.6 μm CMOS process [16]. The results are shown in Table 3. Spice severely underestimates the noise figure of the LNA. While the noise figure predicted by the model in this paper still underestimates the noise of the

LNA, the author stated that there were other sources of noise outside of the amplifier that added to the noise figure, such as board parasitics as well as noisy bias components. The author further stated that the prediction of the model presented here is similar to the noise figures presented in similar CMOS LNA's.[4]

Table 3. LNA Noise Figure Predictions and Measurements

Spice	This Model	Measured
2.6 dB	3.4 dB	5 dB

IV. Conclusion

A complete model for the drain current noise for MOSFET devices in the saturation region has been presented. This model accounts for mobility degradation, DIBL, CLM, as well as electron temperature. Also, an intuitive model for the noise induced by the substrate current Isub at high drain voltages was presented. These models were shown to match well with observed noise data presented in earlier papers.

From these models, a few key guidelines can be extracted. The models in this paper, as well as the observed data, indicate a severe increase in the noise at high electric fields, making it imperative that as device geometries are reduced, terminal voltages must be reduced as well, to minimize the electric fields existing in the channel. Also, in order to achieve a minimum amount of noise, the device should be biased at low (V_g-V_t) in order to keep the device acting as a long-channel device. In addition, the (V_g-V_t) should be small enough to avoid the peak in the I_{sub}-V_g curve.

V. References

1] A. Karanicolas, "A 2.7V 900MHz CMOS LNA and Mixer," ISSCC Digest of Technical Papers, February 1996.

[2] A. Shahani, D. Shaeffer, and T. Lee, "A 12mW Wide Dynamic Range CMOS Front-End for a Portable GPS Receiver," ISSCC Digest of Technical Papers, February 1997.

[3] A. Abidi, "High-Frequency Noise Measurements on FET's with Small Dimensions," IEEE Transactions on Electron Devices, vol. ED-33, no. 11, pp. 1801-1805, November 1986.

[4] D. Shaeffer and T. Lee, "A 1.5V, 1.5GHz CMOS Low Noise Amplifier," 1996 Symposium on VLSI Circuits, p. 32-3, June 1996.

[5] R. Jindal, "High-Frequency Noise in Fine Line NMOS Field Effect Transistors," International Electron Devices Meeting, pp. 68-71, December 1985.

[6] P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd Edition, John Wiley & Sons, Inc., New York, 1993.

[7] S. Wolf, *Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET*, Lattice Press, California, 1995.

[8] Z. Liu, C. Hu, J. Huang, T. Chan, M. Jeng, P. Ko, and Y. Cheng, "Threshold Voltage Model for Deep-Submicrometer MOSFET's," IEEE Transactions on Electron Devices, vol. 40, no.1, pp.86-93, January 1993.

[9] B. Wang, J. Hellums, and C. Sodini, "MOSFET Thermal Noise Modeling for Analog Integrated Circuits," IEEE Journal of Solid-State Circuits, vol. 29, no. 7, pp. 833-5, July 1994.

[10] R. Jindal, "Noise Associated with Substrate Current in Fine-Line NMOS Field-Effect Transistors," IEEE Transactions on Electron Devices, vol. ED-32, no. 6, pp. 1047-52, June 1985.

[11] B. Wang, "Wide Band Noise in MOSFETs," M.S. Thesis, Massachusetts Institute of Technology, October 1992.

[12] A. Van der Ziel, *Noise in Solid State Devices and Circuits*, John Wiley & Sons, Inc., New York, 1986.

[13] K. Seeger, *Semiconductor Physics*, Springer-Verlag, New York, 1973.

[14] R. A. Smith, *Semiconductors*, Cambridge University Press, New York, 1978.

[15] G. W. Taylor, "Velocity-Saturated Characteristics of Short-Channel MOSFETs", AT&T Bell Laboratories Technical Journal, Vol. 63, No. 7, September 1984.

[16] J. Rudell, et. al., "A 1.9 GHz Wide-Band IF Double Conversion CMOS Integrated Receiver for Cordless Telephone Applications," ISSCC Dig. Technical Papers, Feb. 1997.