

Reliable, High-Performance I/O Buffer Design for Multiple Power Supply Systems

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Abstract: In IC designs which incorporate multiple power supply voltages, the interfacing of signals between blocks with different power supplies can be achieved through I/O buffer circuits, which demand high-performance as well as ESD protection for the inputs and outputs. High performance buffers are also desirable for intra-chip interfacing for technologies that require multiple supply voltages. This work presents a set of buffers suitable for use in multiple power supply systems. The intra-chip buffers presented are low-area, high-speed buffers able to convert between the voltage levels of differing power supplies. The inter-chip buffers presented are high-speed buffers which can withstand voltages on bus lines of up to twice the chip power supply, with exceptionally good performance when compared with comparable work in literature. However, the investigation of ESD protection was less successful. A method of designing ESD protection for these multiple voltage systems is described; however, this is a relatively standard method of ESD protection. Overall, however, a significantly faster buffer design is developed for use in multiple power supply systems.

I. Introduction and Background

Aggressive scaling of IC devices, driven by the desire for higher circuit density and faster speed, has increased the functional complexity of VLSI circuits. This has in turn reduced the minimum feature sizes of transistors, requiring a lowering of the power supply voltage in order to maintain safe and reliable device operations. Moreover, power consumption constraints have driven voltages down as well.

One of the key dimensions that is being scaled in high-performance technologies is the oxide thickness t_{OX} . A device's drive capability is inversely proportional to its oxide thickness; however, as t_{OX} is decreased, the maximum voltage that can be sustained across that oxide is decreased as well. The electric field across the oxide, E_{OX} , is given by

$$E_{OX} = \frac{V_{OX}}{t_{OX}}. \quad (1)$$

As the oxide thickness decreases, the peak voltage across the oxide decreases, as E_{OX} must always remain less than a critical electric field at which the oxide breaks down and starts

to conduct current. As a result, the peak sustainable voltage across the device, which sets the upper bound on V_{DD} , also decreases. As power supply voltages scale, it is quite possible that chips with differing power supply voltages will be used together, in order to minimize cost or other parameters. However, the chip with the higher V_{DD} could potentially cause damage to the chip with the lower V_{DD} due to high gate oxide stresses while the two chips interface. As a result, the inter-chip buffering must be able to prevent the devices on the lower chip from oxide breakdown, as well as utilize the signals from the other chips.

Moreover, the requirements for power-efficient and energy-efficient computing are driving power supply voltages down, even in situations when such an increase is not mandated by technology limitations. Since

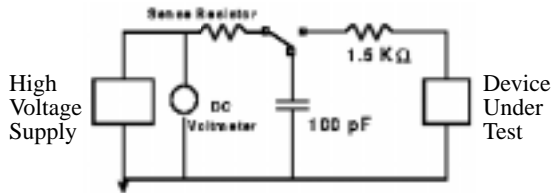
$$P = V_{DD}I_{SUP}, \quad (2)$$

where I_{SUP} is the current drawn from the supply, an obvious method of reducing the power consumption is to reduce V_{DD} . It is well known, however, that reducing the supply voltage without scaling the device increases the propagation delay, to first order, while reducing the power supply voltage as the device as scaled can maintain a constant delay[1]. As a result, certain blocks may no longer be able to function at lower voltages. One solution to this problem is to support different V_{DD} 's for different blocks on the same chip, i.e., use a higher supply voltage for a high-speed block, but use a lower supply voltage for a slower block, which reduces power consumption. While oxide breakdown is not a problem when interfacing blocks on the same chip (all the supply voltages used on chip should be within the normal range of allowable voltages), communication between the two blocks becomes important. As a result, intra-chip buffering is required to convert signals running between the blocks into ones understandable by both.

Another significant effect that must be considered is the response of the buffer circuit to an ESD event. Electrostatic discharge (ESD) is a pervasive reliability concern in VLSI circuits [5]. It is a short duration (< 200 ns) high current (> 1

A) event that causes irreparable damage to all categories of IC devices. The most common manifestation is the human body model (HBM) ESD event, where a charge of about $0.6 \mu\text{C}$ can be induced on a body capacitance of 100 pF , leading to electrostatic potentials of 4 KV or greater. The equivalent circuit for the HBM is given in Fig. 1.

FIGURE 1. The Human Body Model of an ESD Event



As shown in this figure, the 100 pF capacitor can be charged by a high voltage power supply through the switch and then on contact to a device can discharge through the $1.5 \text{ K}\Omega$ equivalent resistor for the human body. This will cause a peak current equal to the ratio of the peak voltage to the $1.5 \text{ K}\Omega$ resistor to flow through the device in a very short time. The device impedance is negligible under ESD. The short duration ($\sim 110 \text{ ns}$) high current ($\sim 1.3 \text{ A}$) pulse can cause insulator breakdown and thermal damage of Si and interconnects including contacts and vias [3,11,12]. Thus ESD protection circuitry must be investigated and incorporated into any robust I/O buffer design.

Previous work which addresses this buffering issue is limited [4,6,8], and has significant problems. All are slow, with propagation delays in the 2.75 ns [4] to 5 ns [8] range. Moreover, [4] requires depletion mode devices, making it unsuitable for many standard processes.

In this work, a new buffer design is presented that deals with the problems mentioned earlier, as well as an ESD structure that is suitable for such a purpose. The next section deals with the design of the buffer circuitry, first presenting the intra-chip buffer design, and then explaining the new inter-chip buffer design. In the following section, results are presented along with comparisons to comparable work. In section IV, on page 7, the details of ESD structures are discussed, including the reasons for difficulty in implementing ESD as well as the final structure that was decided upon. Finally, Section will conclude this paper. For those with interest, Appendix A is included at the end of this paper in order to discuss the limitations of the inter-chip buffer design presented.

II. Buffer Circuit Design

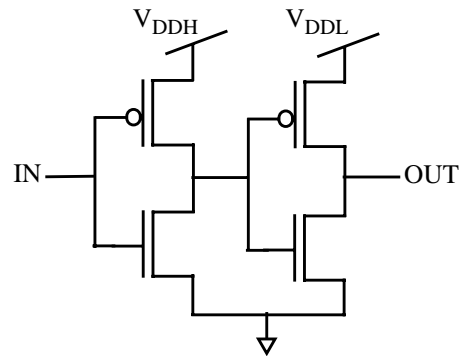
In this section, both the intra-chip as well as inter-chip buffers will be presented, and each will be detailed as to its mode of operation.

A. Intra-chip Buffer Design

In the case of multiple power supply voltages driving different blocks on the same chip, a buffer must be designed that can convert signals between the two blocks. An important point to note here is that since both blocks will normally be tied to the same electrical ground, the only difference between the signal levels will be for the voltage representing a '1', or V_H . Once this point is seen, the conversion buffers are very simple and straightforward.

For the intra-chip buffer design, it is not necessary to limit the voltage drop across the gate-oxide; all of the power supply voltages used on chip will be less than the voltage needed to cause oxide breakdown. As a result, the only issue is that of the level conversion, of which there are two different cases: (1) converting from a block with a higher V_{DD} (and thus a higher V_H) to one with a lower V_{DD} , and (2) converting from a block with a lower V_{DD} to one with a higher V_{DD} . The two cases are not the same, as in the former case, the higher V_{DD} will guarantee that the PMOS device in an inverter will be turned off (as it will ensure that the V_{gs} of the PMOS is greater than 0, keeping it off) and ensuring proper inverter behavior. However, in the latter case, the lower V_{DD} can keep the PMOS device of an inverter on even when the input is supposed to be high, potentially causing an unknown value at the output of this inverter.

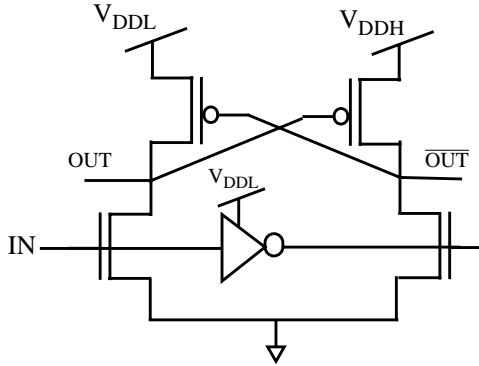
FIGURE 2. High-Low Intra-Chip Conversion Buffer



Case (1) will be examined first. The circuit shown in Fig. 2 converts quickly from voltage levels in the higher V_{DD} block to those in the lower V_{DD} block. If the input is a '0', the intermediate node is inverted to the '1' level of V_{DDH} , which is then inverted to a '0' again by the second inverter (since

V_{DDH} is larger than V_{DDL} , the PMOS device in the second inverter is shut off, and thus OUT is sunk to '0' by the NMOS device. In the case of the input being a '1', the intermediate node is at logic level '0', which is common, and the output sits at the level '1' of the lower V_{DD} block V_{DDL} . Sizing is not really an issue here, as these are standard inverters, with no devices being on at the same time and creating conflicts at a certain node.

FIGURE 3. Low-High Intra-Chip Conversion Buffer



In Case (2), the circuit from Fig. 2 cannot be used, since if the input was the high voltage of the block with the low V_{DD} , it is possible for both the NMOS and PMOS devices of the first inverter to be on simultaneously if

$$V_{DDL} < V_{DDH} - |V_{tp}|, \quad (3)$$

causing static power dissipation, as well as creating logic uncertainties at the intermediate node. Another technique must be used to ensure proper conversion. Fig. 3 shows a different buffer, which uses the positive feedback of the cross-coupled PMOS devices to force the outputs to go the supply and ground rails, and create adequate conversion. The key issue in the design of this circuit, is that the devices must be sized large enough so that the side that sees V_{DDL} as its input will start to make the transition, i.e. the NMOS device on that side must be sized large enough that its drain starts to go low. Once that node starts to go low, the positive feedback will force the circuit to its final static state. This is also a very fast circuit, as the positive feedback enhances the speed of the circuit.

In fact, this circuit can be used for both the high-low as well as low-high conversions; however, one may want to consider the circuit presented in Fig. 2 for the high-low case, as it consumes less power (two inverters rather than three).

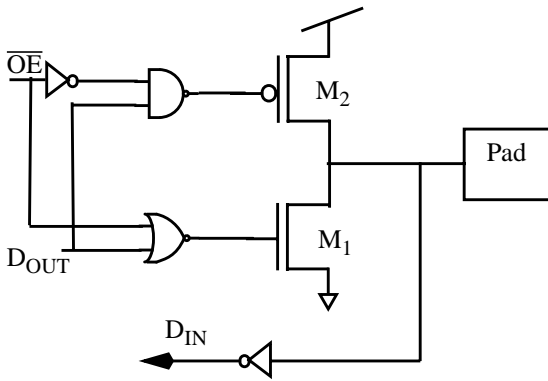
B. Inter-Chip Buffer Design

The real interesting circuit design occurs in this circuit. The previous section detailed buffer circuits that are relatively well known. They are fast, and need only be as big as needed to drive their particular load capacitances. However, in the inter-chip buffer design case, there are some very important limitations. First, these buffers must be able to drive large capacitive loads, as they are driving off-chip signals, which means driving I/O pads, parasitic board capacitances, and capacitances on other chips. Second, as stated in Section I, the voltage across any oxide at any time should not be greater than the supply voltage, which ensures oxide reliability; most process design engineers will not guarantee oxide reliability for oxide voltages greater than the chip V_{DD} . If a low voltage chip is tied to a bus which connects several chips, some with higher supply voltages, then the I/O buffer must be designed such that there is no chance of a problem with the oxide.

There has been very little work in this area, surprisingly. The work that has been done is relatively complex, and in that complexity, causes problems which can slow the circuit down. Fig. 4 shows a standard I/O buffer configuration, for the case of a system with a single power supply. The buffer is designed to be driven only when the output enable signal \overline{OE} is asserted. Clearly, this needs to be modified if the pad voltage can go above the chip V_{DD} when the output part of the buffer is disabled. First, the voltage across the oxide of the NMOS at the drain end will be above the chip V_{DD} , and thus problematic. Second, if the pad voltage rises above $V_{DD} + |V_{tp}|$, then the PMOS device turns on, and the PMOS device conducts back into the supply. Finally, the drain-bulk pn junction of the PMOS device can get turned on if the pad voltage rises above $V_{DD} + V_{diode}$, where V_{diode} is the turn-on voltage of the diode. All these concerns must be addressed.

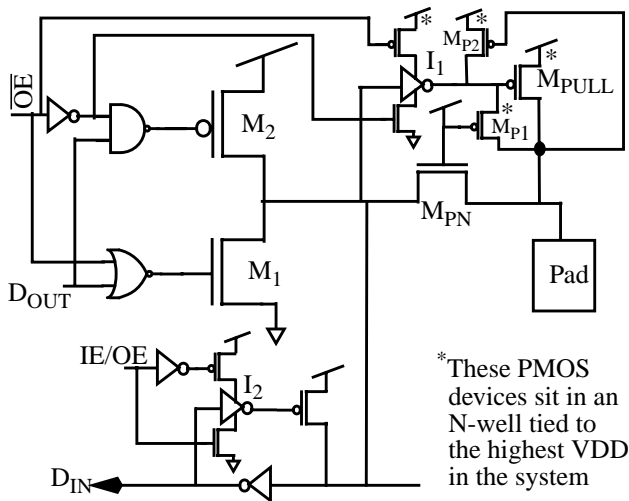
The methods used in the literature to date [4,6,8], are adequate and solve all of the above problems; however, the methods used tend not to utilize the advantages particular to this output circuit, and as such, suffer performance problems. These works tend to put extra circuitry both before and after the final inverter shown in Fig. 4. However, that tends to slow down the arrival of the signal to the input of the final inverter, which is added to the extra delay of the circuitry between the pad and the base inverter. What should be realized is that the final inverter in Fig. 4 is large enough to drive a very large capacitive load (on the order of 20 pF); adding a few picofarads of capacitance at the output node is really inconsequential, and shouldn't significantly degrade the propagation delay through this structure. Therefore, the emphasis should be on trying to put as much of the extra circuitry as possible after the M_1 - M_2 inverter.

FIGURE 4. Standard I/O Buffer Configuration



A new circuit which solves the problems listed above is shown in Fig. 5. The first point to note is that all of the new circuitry is placed *after* the driving inverter, which means that all of that excess capacitance (due to the extra devices incorporated into the design) will be driven by a very large size inverter (M_1 - M_2), which is already driving a much larger capacitance, minimizing extra delays in driving the output. More importantly, the added circuitry should not cause any significant modifications in the design of the previous stages. The previous stages see exactly the same buffer as in the standard situation; the buffer chain driving the final buffer need not be resized.

FIGURE 5. New I/O Buffer with High Voltage Protection



Secondly, the only device between the inverter and the pad is the NMOS pass transistor M_{PN} . The PMOS pull-up device is needed to offset the V_m signal loss through the pass transistor for an output high; however, the signal will rise to a significant percentage of its final value before the PMOS device is really needed. The PMOS pull-up is operated through a feed-

forward procedure; the output signal is inverted by the inverter I1, which drives the PMOS pull-up, and ensures that the pull-up works when it is supposed to. The inverter is enabled using extra devices which turn the inverter on only when the output is to be enabled. Thus the output buffer performs well as an output buffer; there is little circuitry in the signal path that could slow it down, unlike previously reported versions.

When the output portion of the buffer is disabled, it is possible for other chips to grab the bus and assert signals which are larger than the chip V_{DD} . The pass transistor M_{PN} is the crucial protection device, as it limits the voltage that the driver inverter sees to a V_t drop below the chip V_{DD} , which poses no threat to gate oxides. The pass transistor itself is immune from problems relating to oxide breakdown, since its gate is biased at the chip V_{DD} , and can allow its drain to go as high as twice the chip V_{DD} without problem. Thus the devices that make up the main signal path - M_1 , M_2 and M_{PN} , are all safe from any oxide breakdown effects.

Because the pass transistor limits the voltage at the output of inverter made up of M_1 - M_2 , there is no need to protect the device M_2 from reverse conduction. However, the problem has simply been moved to the pull-up transistor M_{PULL} . If the pad voltage goes above V_{DD} , it can start to turn on M_{PULL} . A solution that was presented in [8] is a very simple and effective one. The transistor M_{P1} is added to raise the voltage of the gate of M_{PULL} as the pad voltage increases. M_{P1} will ensure that the gate of M_{PULL} remains a $|V_{tp}|$ drop below the pad voltage, keeping transistor M_{PULL} off. However, once the pad voltage returns to a logic level of '0', there is no way for the gate to discharge, and so there is the potential for a voltage larger than the chip V_{DD} across that gate oxide (the gate-drain of M_{PULL}). Thus M_{P2} is added, which senses when the output returns to its low state, and returns the gate of M_{PULL} to the chip V_{DD} .

One other problem mentioned earlier was that of forward biasing the drain-bulk junctions of PMOS devices whose drains rose above the chip V_{DD} . This is simply solved by bringing the highest VDD in the system on chip, and using that voltage to bias the N-well that those select PMOS devices are built in. The devices in that well are denoted with asterisks in Fig. 5.

Finally, the input buffer portion of the circuit also works quite simply. The chip side of the pass transistor is sensed and inverted (if the input enable signal is active), and a PMOS pull-up device is used to raise the voltage to its full level in the case of a logic '1'. Not shown (for clarity's sake) is another PMOS device that will charge the node

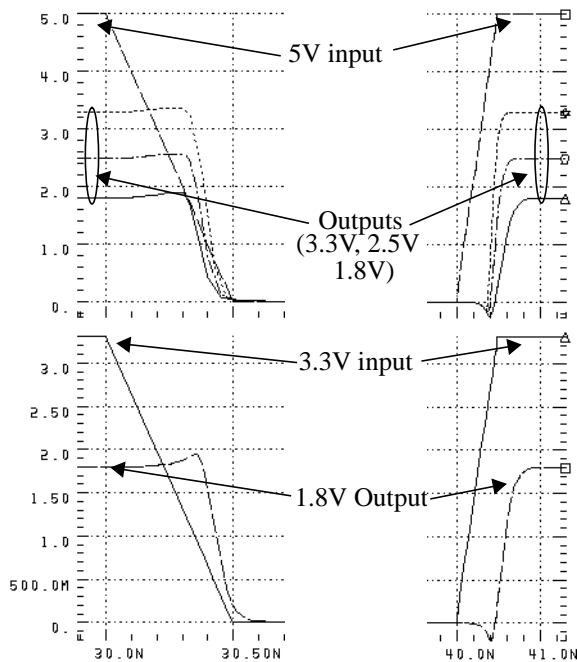
labeled D_{IN} to V_{DD} when the input enable signal is inactive, so the PMOS pull-up remains off.

The above circuit is a simple but effective way of buffering signals that need to be driven to the output, while at the same time preventing the devices from suffering from any potential oxide breakdown events that might happen. The next section will show the results from simulation, as well as comparisons to the previous work mentioned earlier.

III. Buffer Design Results

In this section, results from simulations of the buffer circuits will be shown, and these results will be compared with published data (as limited as it is). First the intra-chip buffer simulations will be examined, after which the simulations of the inter-chip buffer will be presented.

FIGURE 6. High-Low Conversion Buffer Simulation Results



The high-to-low level conversion buffer simulation results are shown in Fig. 6, which shows a very quick conversion from the higher level to the lower level. The final stage was loaded down with a capacitor approximately five times greater than its own capacitive input. Still, the conversion is very quick - in fact, the low to high transition is almost instantaneous! This is most likely due to the heavy overdrive on the gate of the second NMOS, which is driven with a 5 V signal. The low to high delay is slightly longer, but still quite fast. Fig. 6 shows the high-to-low transition of the input (V_{DDH}) and the output (V_{DDL}) on the left and the low-to high transitions on the right.

The operation of the low-to-high level conversion buffer is shown in Fig. 7. The graph shows conversions from 1.8 V to both 5 V and 3.3 V. Again, the transitions are very fast. The data for the speed of the intra-chip buffers is given in Table 1. The buffers all have delays of less than a nanosecond, making them very attractive for this conversion process.

FIGURE 7. Low-High Conversion Buffer Simulation Results

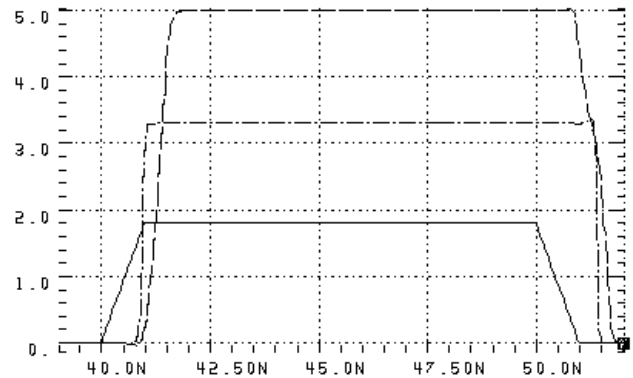


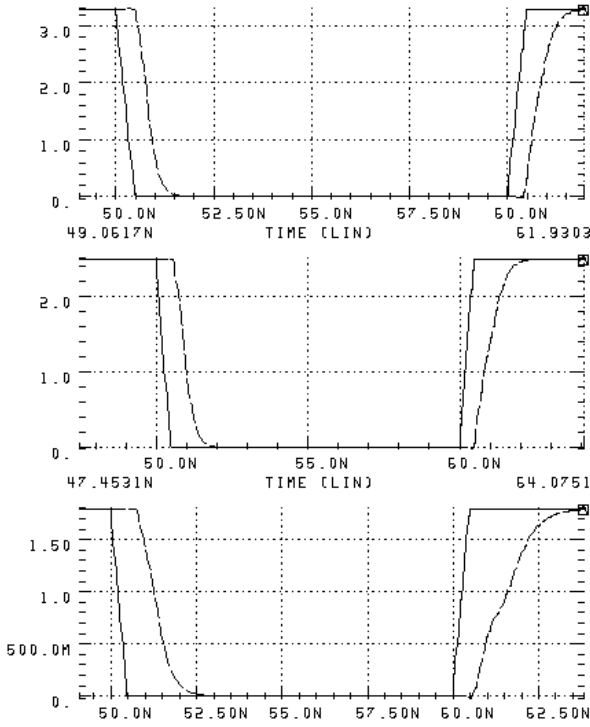
Table 1. Intra-Chip Buffer Performance

$V_{DD1} \rightarrow V_{DD2}$	t_{PLH} (ns)	t_{PHL} (ns)
1.8V \rightarrow 5V	0.825	0.984
2.5V \rightarrow 5V	0.498	0.494
3.3V \rightarrow 5V	0.353	0.337
1.8V \rightarrow 3.3V	0.635	0.691
5V \rightarrow 1.8V	0.330	0.124
5V \rightarrow 2.5V	0.238	0.135
5V \rightarrow 3.3V	0.195	0.146
3.3V \rightarrow 1.8V	0.331	0.194

The results of the inter-chip buffer are equally encouraging, especially when compared with the previous published results. The inter-chip buffer was laid out in a MOSIS 0.5 μm (L_{eff}) process. The layout was not completely optimized; it is quite likely that a competent layout tech could reduce the area significantly, but the layout indicated a 25% to 50% area penalty to implement the buffer. The layout is shown in Fig. 17, at the end of this paper. Fig. 8 shows the output as it operates in the output buffer mode (\overline{OE} is enabling the output buffer). The data signal D_{OUT} is the first signal to rise and fall, and the following signal is the output at the pad. The three different plots represent chip power supplies of 3.3 V, 2.5 V, and 1.8 V, respectively. As can be seen, the signals follow without much delay. As the chip VDD goes lower, the delay starts to increase, as would be expected; however, if the process were to scale with the supply, this decrease in performance would not be noticed, as the increased drive capability of the devices would

compensate for the lower supply voltage. Even accepting the fact that these delays are not optimum as the VDD decreases, the performance of the buffer still is significantly better than that shown in [4,8], as the results in Table 2 show. The results were obtained with the buffer driving a 20 picofarad load, which seemed to be a common metric in the literature (one of the papers used as a comparison used 22 pF, one used 20 pF).

FIGURE 8. Results of Inter-Chip Buffer Output Simulation



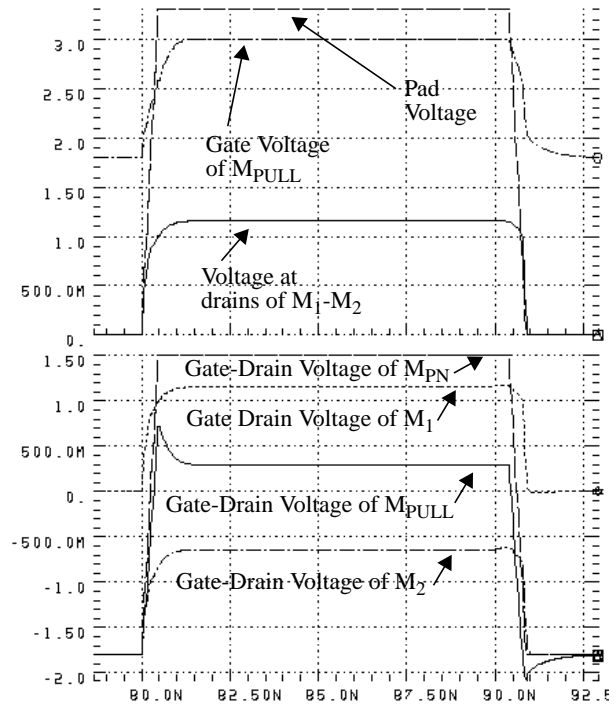
The buffers were optimized for 1.8V (the driver devices M1 and M2 were sized at $500\mu/0.6\mu$ and $1000\mu/0.6\mu$, which was suggested to be a relatively standard size pad driver for 1.8V). At 2.5V and 3.3V, the speed-up over the delays from the two references is significant; it must be noted, however, that the drivers would likely be down-sized as the power supply voltage is increased, in order to save on area and power. Still, the increase in speed is definitely very large. Moreover, since the design of the ESD was not as successful as hoped, it could not really be incorporated into the design as desired. As a result, the propagation delay simulations were redone with a higher load capacitance value of 30 pF (instead of 20 pF) in order to account for the ESD diodes. Still it can be seen that the circuit provides extremely good performance, even at the low supply voltage of 1.8 V.

While the increase in speed is large, the issue of protection must still be simulated as well. This was done by disabling the output function of the buffer, and applying a voltage signal

Table 2. Inter-Chip Buffer Performance

Chip VDD	t_{PLH} (ns), 20pF	t_{PHL} (ns), 20pF	t_{PLH} (ns), 30pF	t_{PHL} (ns), 30pF
1.8V	1.24	1.08	1.47	1.24
2.5V	0.71	0.71	0.856	0.819
3.3V	0.524	0.578	0.631	0.668
Pelgrom [8], 3.3V	3.6 ns	4.1 ns	N/A	N/A
Toshiba [4], 3.3V	3 ns	2.5 ns	N/A	N/A

FIGURE 9. Results of Applying High Voltage signal at I/O pad (Chip VDD=1.8V, Off Chip Signal = 3.3V)

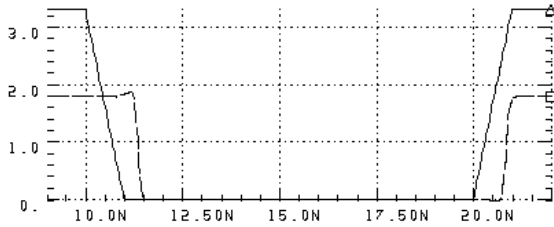


that swung between ground and the higher off-chip voltage. While the pad voltage runs between 0 and 3.3V for the case shown, the voltage across any portion of the oxide of any of the devices that might see a high voltage is limited to 1.8V, which is the chip VDD. As stated in Section II, the pass transistor limits the voltage across the oxides of M1 and M2 as well as it's own, and the devices M_P1 and M_P2 prevent the reverse conduction of M_PULL.

Finally, the results of simulating the input buffer portion of the I/O buffer are shown. Again, as this is a relatively simple buffer, it offers very good performance and very little delay. The results are shown in Fig. 10, which shows very good performance for the conversion of a 3.3V input signal

to a 1.8 V signal at D_{IN} with no oxide failure problems, since the input to the input buffer is held at a threshold voltage below the chip V_{DD} . The input side of the buffer has propagation delays of 0.35 ns for t_{pLH} and 0.87 ns for t_{pHL} .

FIGURE 10. Simulation of Input Path of I/O Buffer



The buffers designed for this work have been described, and the results that have been derived meet the design guidelines very well. They are fast, and easily match and better the performance of previously published work.

IV. ESD Protection Issues

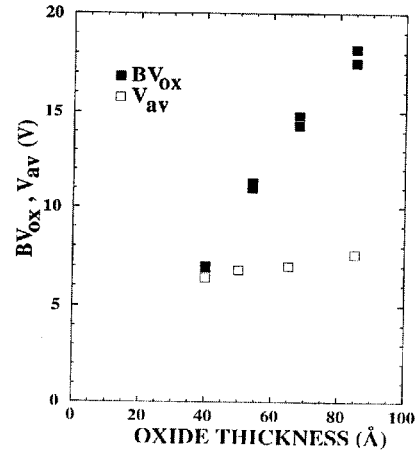
Scaling of VLSIC devices have reduced the dimensions of all structures used in the ICs and this has increased their susceptibility to ESD damage [13]. Hence ESD protection issues are becoming increasingly important for deep sub micron technologies. The gate oxide thicknesses are approaching the tunneling regime of around 35 angstroms. From an ESD perspective, the important issue is whether the oxide breakdown is reached before the protection devices are able to turn on and protect them [10]. Hence, the avalanche breakdown voltage V_{av} and the oxide breakdown voltage BV_{OX} are the important parameters to monitor. A more relevant parameter is the margin between V_{av} and BV_{OX} given by $(V_{av} - BV_{OX}) = \Delta V_{trig}$. As this margin gets smaller protection of devices will become more difficult. Fig. 11 shows the dependence of V_{av} and BV_{OX} on the gate oxide thickness between 40 angstroms and 85 angstroms [13]. It can be observed that as the oxide thickness approaches 40 angstroms, ΔV_{trig} approaches zero, indicating that this will become a critical issue for sub 0.25 μm technologies.

A. ESD Design Options

Although good protection designs have been common from 2 μm down to 1.2 μm technologies, device scaling towards deep sub micron regime are causing concerns about maintaining the protection levels for reliability. The important reliability concerns are associated with thinning of gate oxides, scaling of metal interconnect lines including contacts and vias and the various process impacts. In addition, the ESD protection

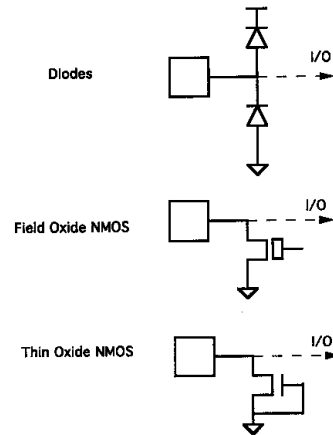
network for buffers interfacing between multiple chips presents other constraints that needs to be addressed as well.

FIGURE 11. Oxide breakdown voltage, BV_{OX} , and the junction avalanche voltage, V_{av} , as a function of oxide thickness for 200 ns stress pulses.



We examined three common ESD design options. These designs are summarized in Fig. 12. The thick field NMOS design is clearly not suitable for deep sub micron processes, and the thin field oxide NMOS presents oxide breakdown problems while interfacing between blocks with high power supply voltages.

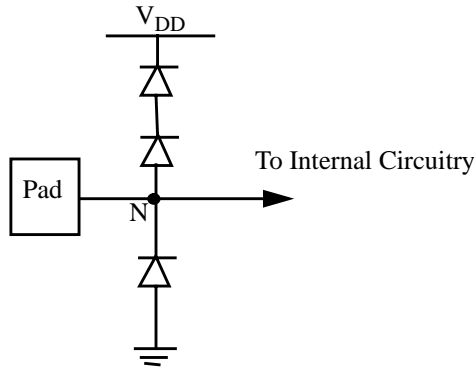
FIGURE 12. Common ESD protection device options.



Thus the protection scheme with the diodes is used in the interfacing I/O buffer circuit. Fig. 13 shows a schematic of the proposed ESD protection scheme. The forward biased diodes connected to VDD simply serves to shunt the ESD current during a discharge condition. The reverse biased diode is provided for the negative pulse. An important consideration in the ESD protection circuit for I/O buffers interfacing between different multiple supply voltages is the

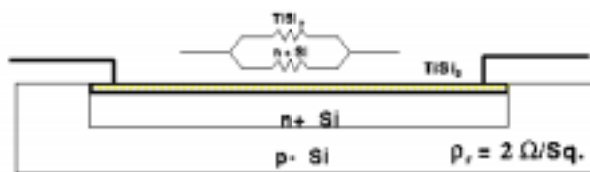
fact that the ESD circuit should not be allowed to clamp the voltage at the node N shown in the Fig. 13, below the voltage at the pad. To overcome this problem the diode chain is proposed. In the reverse direction a single diode is sufficient, since the reverse breakdown voltage is usually much higher (~ 5 V).

FIGURE 13. Proposed ESD Protection Scheme



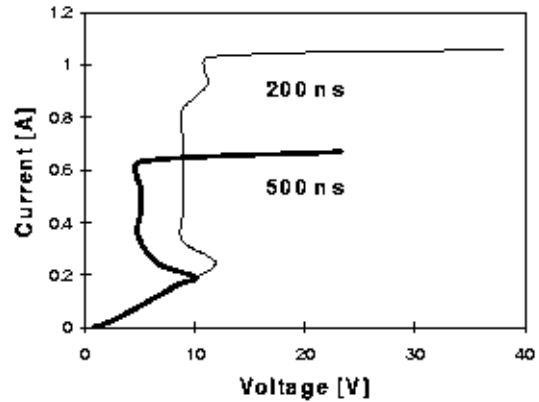
We have also investigated the option of connecting a low resistance (~ 1 Ohm) between the pad and the node N. Introducing this resistor would doubly ensure that the ESD discharge path will not activate under normal voltage swings at the pad at the slight cost of increased power dissipation. Various resistor design options were examined. These designs included a simple n-well resistor, silicide block resistors and silicide clad n-contact resistors. A transmission line technique [14] was used to generate constant current pulses to stress the various resistor structures. The silicided n-contact structure was found to be more suitable for the purpose of providing a small resistance between the I/O pad and node N. Fig. 14 shows a schematic of the n-contact resistor structure with L/W = 5/5 and a sheet resistance of 2 Ohms/Sq. The corresponding I-V curves for a 200 ns and a 500 ns pulse is shown in Fig. 15. An interesting point to note in Fig. 15 is that the impact ionization effect in the semiconductor is more severe for the shorter pulse width. This results from the decreasing heat diffusion time into the semiconductor under shorter stressing pulses. The heating effect thus increases with shorter pulse width.

FIGURE 14. N-Contact Resistor Structure



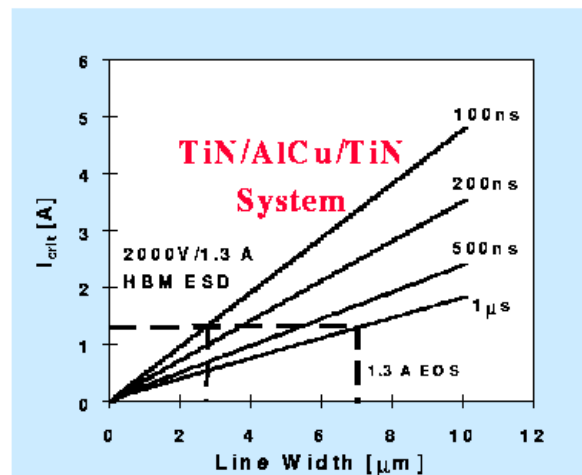
We have also considered the optimization of the I/O buffer interconnects under short duration high current pulsed stress conditions using an interconnect heating model proposed in [15]. Fig. 16 presents a plot of the maximum allowable current I_{crit} vs. minimum required line width under ESD type stress conditions. When designing the ESD protection, these guidelines must be adhered to in order to minimize metal and contact damage.

FIGURE 15. I-V Characteristic for N-Contact Resistor under Pulsed Stress



Unfortunately, time constraints as well as the lack of a readily available, good diode model prevented the ESD circuit mentioned above from being implemented. However, since the theory has been thoroughly examined, the circuit should be straightforward to implement.

FIGURE 16. Design guidelines for ESD buffer interconnects.



V. Conclusions

In this work, buffer design for systems with multiple power supply voltages has been examined. High performance buffers for single-chip designs with multiple power supply voltages, in which the gate oxide reliability is not an issue, were presented. In addition, an inter-chip I/O buffer was designed that protects low voltage chips from bus signals that may exceed that chips power supply voltage, while maintaining worst case delays of 1.24 ns into a 20 pF load. This advance is significantly faster than previous published works. Finally, the issue of ESD protection was examined, and a protection circuit was designed which incorporated data on N-contact resistors as well as interconnect sizing. The ESD circuit proposed allows the bus voltage to range above the chip's low VDD, while still clamping the voltage at a certain value in the case of an ESD event.

VI. References

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Appendix A. Buffer Limitations

In this section, the limitations of the inter-chip buffer will be described. While they are not numerous, they do limit the instances in which this buffer can be used; moreover, as process trends start to decrease power supply voltages further and further, these issues could be problematic. These limitations only apply to the case of the inter-chip buffer, as the gate oxide reliability must be maintained.

First of all, the use of pass transistors as the device which limits the voltage across oxides puts a limit on the maximum V_{DD} in the system. That is, the voltage applied at the pad cannot be more than twice the chip V_{DD} . If this limit were to be abrogated, the gate-drain voltage across the pass transistor would exceed the chip V_{DD} and cause reliability concerns. As a result, as oxide thickness and supply voltages are scaled lower and lower, the range over which this buffer is usable diminishes. While this is true of the previous implementations as well [4,8], it must be remembered when using this buffer.

Second, the minimum supply voltage that this buffer can be used for is limited to twice the NMOS threshold voltage, again because of the pass transistors. The input side of the I/O inter-chip buffer cannot function below that $2*V_t$ limit. Like CPL [1], low threshold voltage [or zero threshold voltage] devices could be used for passing the signal; however, that no longer makes the function as a protective buffer. With no V_t drop, the entire pad voltage would be passed through to all the devices on the low voltage chip. Since that is not a solution, the limit on the minimum supply voltage must be adhered to.

Third, the inter-chip buffer does not convert its output logic level to a higher level; as such, the chips with higher V_{DD} 's that it interfaces with must be able to resolve the lower value. If the higher V_{DD} chips are also being designed, then the intra-chip conversion buffers presented here could be used to do the conversion. However, if the low V_{DD} chip is meant to be used with an off-the-shelf component running at a higher V_{DD} , the performance of the interface must be thoroughly tested to ensure that the higher V_{DD} chip does not misread bits.

Finally, the extra circuitry in the buffer is large, as shown in Fig. 17, and can add about 25% to 50% to the size of the output buffer. This output buffer was laid out in a MOSIS HP 0.5 μm process, and a very unoptimized layout indicated about a 50% increase in size. While this area penalty can be accommodated for a few pins, that sort of area penalty at each and every pin can be too much to afford.

FIGURE 17. Layout of Output Buffer

