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RF CMOS Class C Power Amplifiers for Portable Wireless Communications

In recent years, the explosion in demand for portable wireless communications devices has fueled an emphasis on research into the implementation of these devices. Increasingly, research has focused on attempts to integrate more and more of the functionality of a radio transceiver onto a single chip. These integration efforts have been motivated by the desire to reduce the overall cost of the mobile unit in addition to lowering the power consumption, and reducing the form factor[1]. CMOS technologies have emerged as one of the leading candidates in which to implement these integrated solutions[1][2], as CMOS is both inexpensive as well as the technology in which much of the digital circuitry is implemented. To date, the integration of the Power Amplifier (PA), the block which amplifies the signal to be transmitted to the required transmit power level, has received less attention than other blocks in the transmit and receive chains. One reason for this is that PA design has, for a long time, been more of an empirical design process in which designers use characterized transistors along with characterized passive devices in a heavy simulation loop in order to achieve the final design. Consequently, other blocks whose operation is somewhat better understood have dominated the research until recently. Second, while advanced CMOS processes can facilitate the design of other moderate and high-frequency blocks, they present several technology barriers to the implementation of PAs. Therefore, the focus of this research is the implementation of RF Power Amplifiers in CMOS technologies.

Many of today's wireless communications systems require the mobile unit to deliver large amounts of power to the antenna; for this reason, the PA can dominate the power consumption of the transceiver. As a result, one of the key performance measures of a PA is the efficiency η, which is the ratio of the power delivered to the antenna to the power drawn from the supply. In general, high-efficiency PAs are achieved at the cost of linearity; fortunately, several communications standards utilize constant-envelope modulation schemes (in which the amplitude of the transmitted signal contains no information), which allow for the use of non-linear PA topologies.

Class A PAs, in which the device used remains in its amplification region for the entire input signal excursion (assuming a sinusoidal input signal), provide high linearity but have poor efficiency (around 30% efficient in practice). Class B and AB PAs, in which the portion of the cycle that the device is on varies from 50% (Class B) to between 50% and 100% (Class AB), provide higher efficiencies at the cost of a reduction in linearity, but still the efficiency can be boosted by using an even more non-linear PA. Therefore, the higher efficiency Class C PA topology is being investigated. The simplified topology of a Class C PA is shown in Figure 1.In a

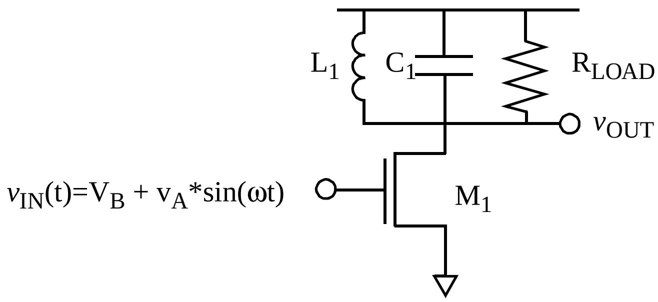

Figure 1. Simplified Class C Power Amplifier Topology

Class C PA, the input signal v_{IN} is biased such that the device is on for less than one half of the input period. This produces a pulsed current waveform in the device. From this, the fundamental frequency component can be extracted using the correct matching network at the output. The Class C PA can achieve higher efficiencies than the Class A, AB or B PAs, as the power consumed in the device is less in the Class C implementation (the I-V product in the device is zero for a greater portion of the cycle). Unfortunately, much of the previous analysis of Class C implementations either assumes the device is always in its amplification region when on [3], or involves heavy state-based equations (essentially transient analysis) in order to model the circuit[4]. A simpler method of analysis to predict the operation of the circuit would be beneficial in the design process. Accordingly, a predictive model for the operation of the Class C PA using a simplified model of the transistor is being investigated.

An additional barrier to the CMOS implementation of the PA are related to the limitations of CMOS technologies. As CMOS processing technology advances, smaller device geometries facilitate the implementation of higher frequency circuits. However, the thinner gate oxides that accompany smaller geometries limit the voltage available at the output. When trying to generate large power levels, voltage swing limitations force the designer to trade current for voltage. As CMOS is generally a poor current drive technology, extremely large devices are required to generate these current levels. These large devices present large capacitive loads to the driving circuits, increasing the difficulty in applying the adequate input signal. Moreover, these loads can become large enough to require inductor values in the tuning networks that are extremely difficult to generate in an integrated system. Another significant problem in integrating the PA in a CMOS technology is the issue of substrate coupling between the PA and other blocks on the same chip. Because of the large current and voltage swings that must be generated in order to deliver the power to the load, the PA will inject large signals into the substrate, which can travel through the substrate and interact with other blocks in the chip. Thus interactions must be limited, or at least injected such that their impact on other blocks in the chip can be reduced. Several circuit techniques, including the use of a differential topology and the use of cascode stages, have been identified as solutions to the technology barriers CMOS presents.

In order to test the design methodology as well as the circuit solutions to the technology barriers, the techniques are being applied to the design of a 250mW PA designed for the DECT system. These techniques will also be used to optimize an existing design, that of a 1W PA designed for the GSM system. The simulation and experimental results will be compared with the design methodology, in order to validate its use in the design of Class C PAs.

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