

Reliable High Performance I/O Buffer Design for Multiple Power Supply Systems

Kaustav Banerjee

R. Sekhar Narayanaswami

EECS 241

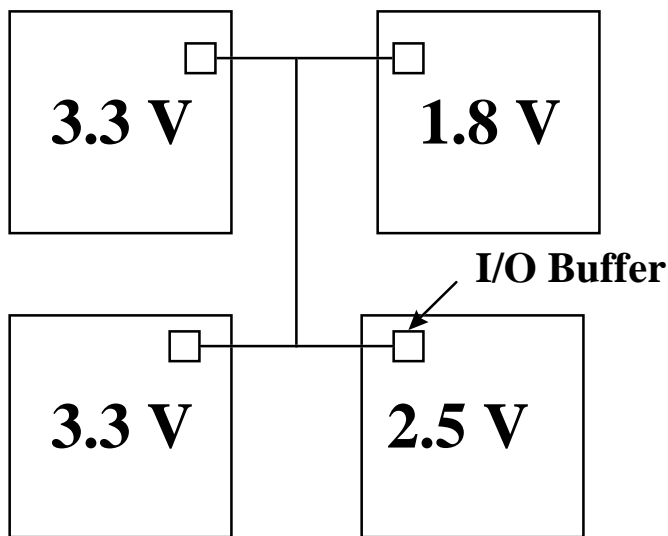
Spring 1997

OUTLINE

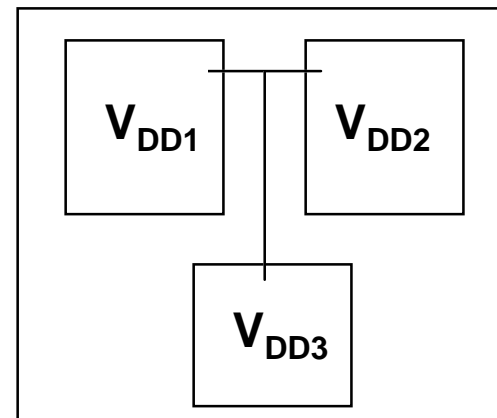
- **Introduction**
- **ESD Protection Issues**
- **Buffer Design**
- **Results**
- **Conclusions**

Motivation

- As VLSIC devices continue to be scaled, **thinner gate oxide** and **lower supply voltages** are making multiple supply systems more common.
- Need **high performance buffers** that can interface between blocks with different power supplies.
- Reliability of the **gate oxide** must be maintained in lower voltage chips.



Multiple Chip Design



Single Chip Design

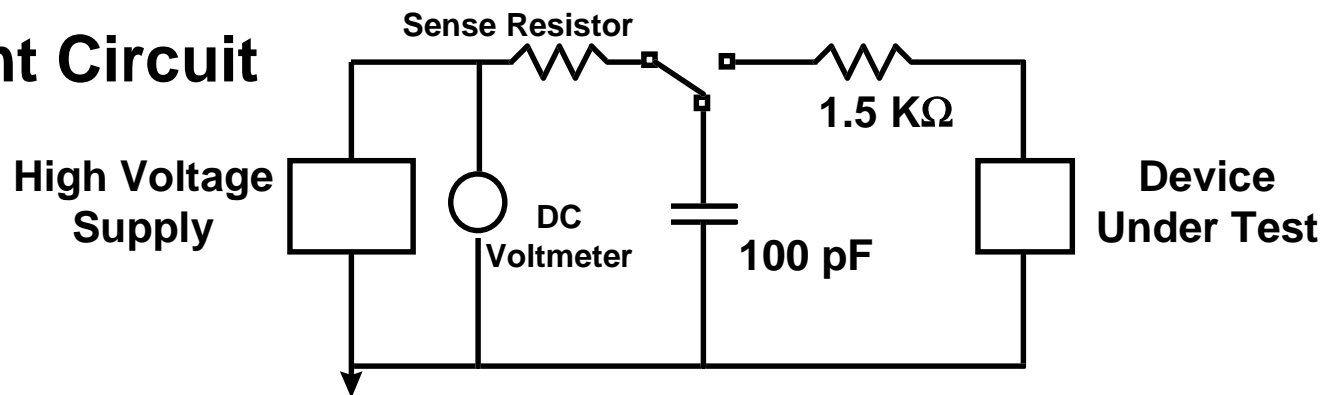
GOALS

- Design **high performance I/O buffer** circuits for intra and inter chip signal interfacing.
- Design a **robust ESD protection** scheme which will allow maximum performance and maintain gate oxide reliability.

Electrostatic Discharge (ESD)

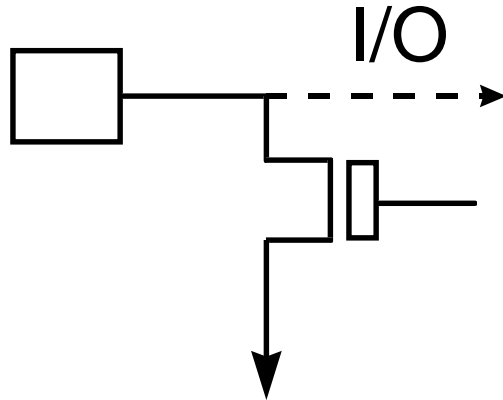
- ESD is a pervasive **reliability concern** in the IC industry and of growing importance for deep sub micron technologies.
- It is a short duration (**10 ns to 200 ns**) high current (**> 1 A**) event that arises on contact from a charged body.
- The high voltages result in large electric fields and high current densities in small devices that leads to **breakdown of insulators** and **thermal damage** in the interconnects, contacts and Si.
- ESD Model: Human Body Model (**HBD**): Humans accumulate charge

Equivalent Circuit

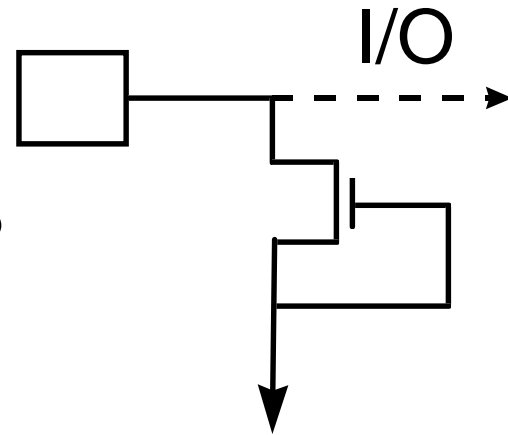


ESD Protection Circuit Design Options

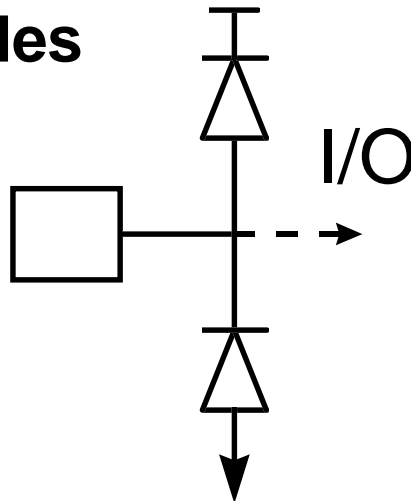
**Thick
Oxide
NMOS**



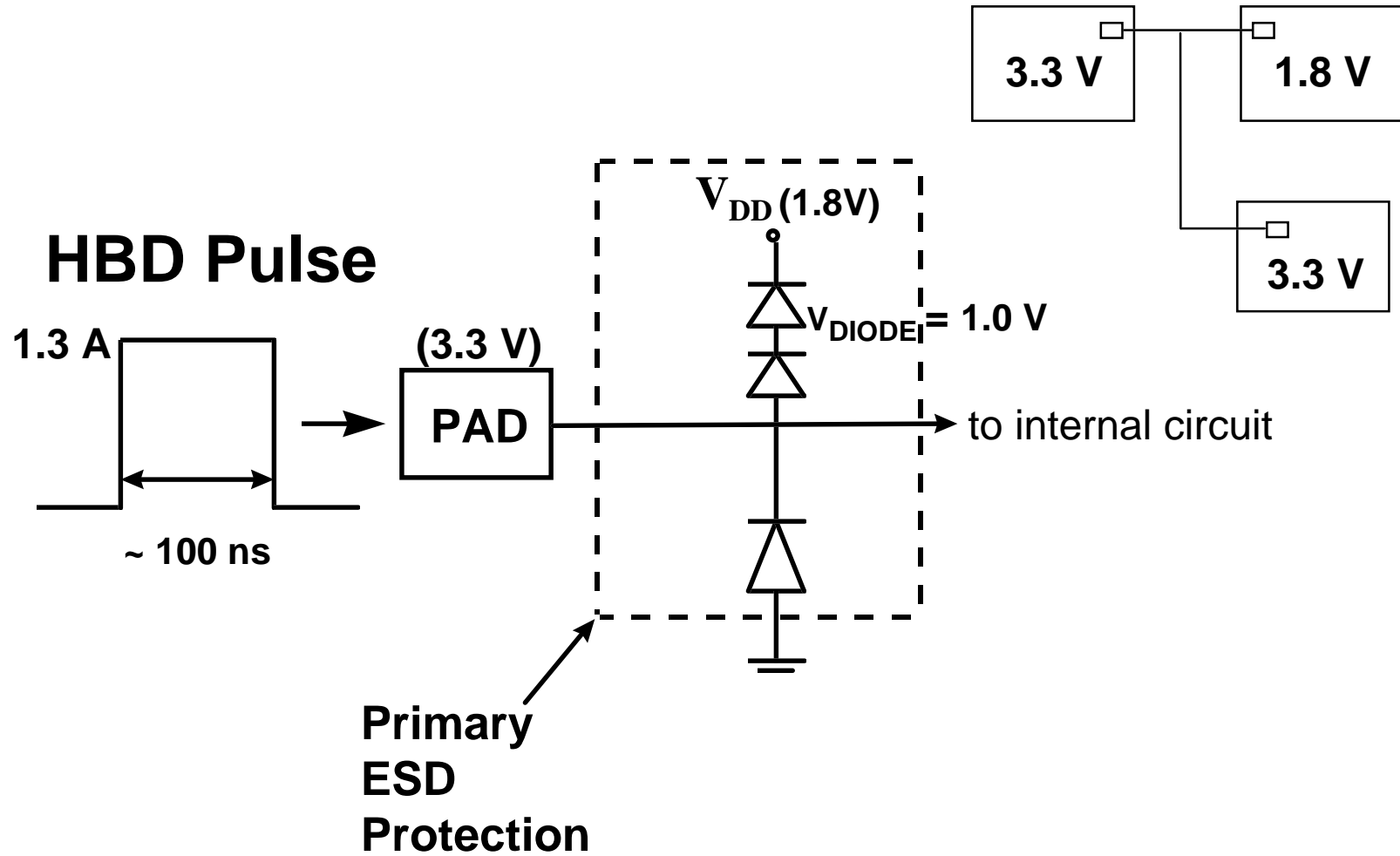
**Thin
Oxide
NMOS**



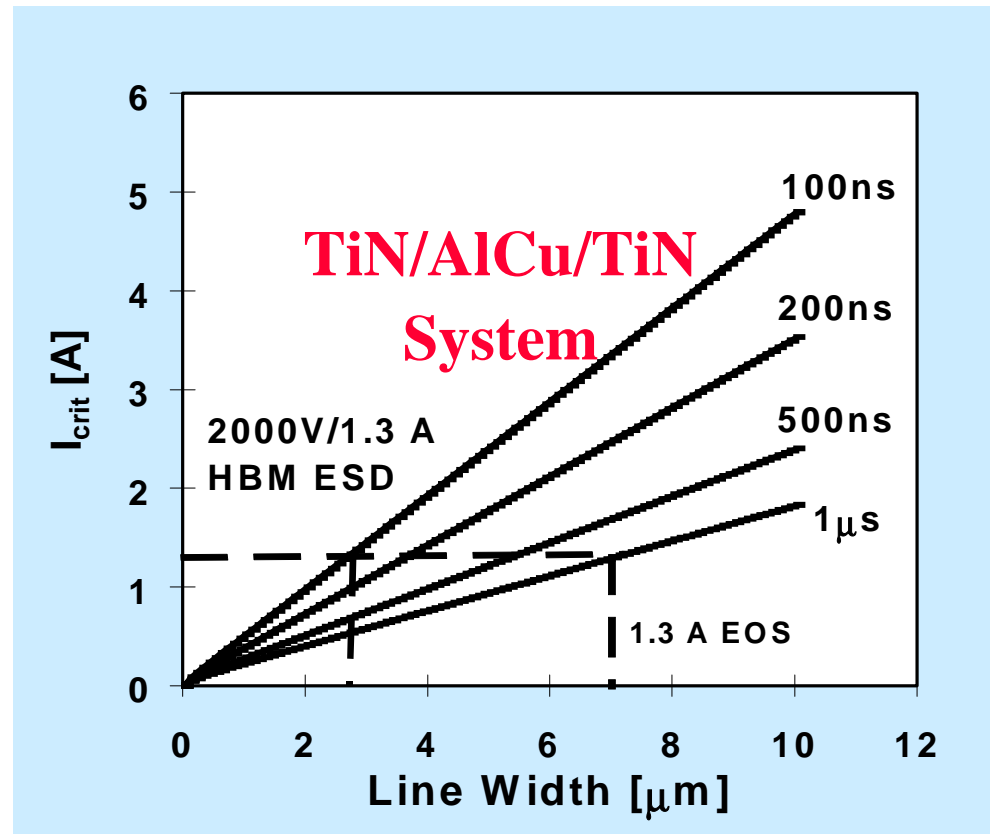
Diodes



ESD Protection Circuit



Design Guidelines for ESD/EOS and I/O Buffer Interconnects

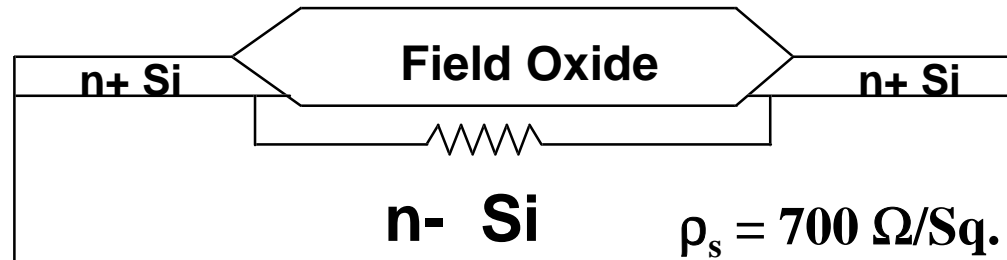


[Banerjee, Amerasekera and Hu, 1996 IRPS]

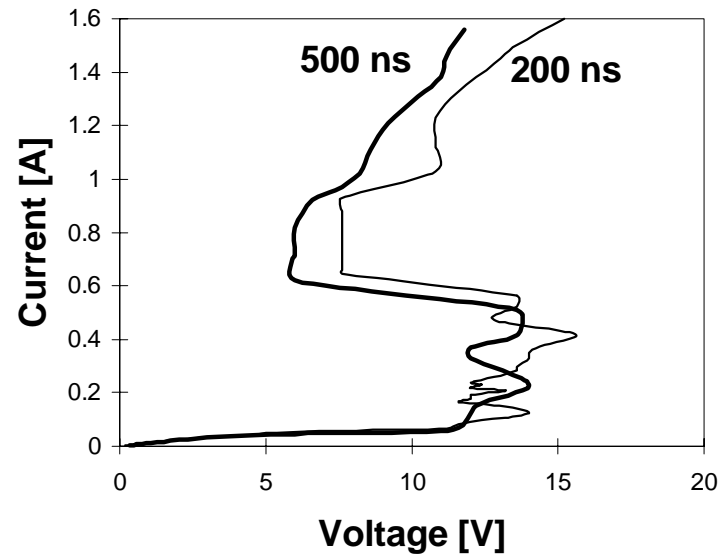
Resistor Design Option-I

N-Well Resistor

$L / W = 2 / 20$



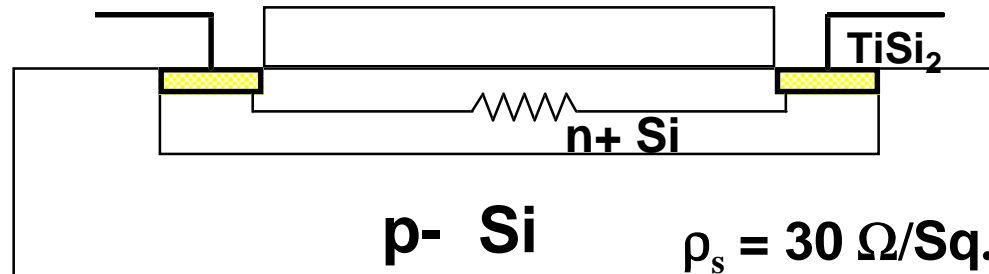
Transmission Line Pulsed Experiment



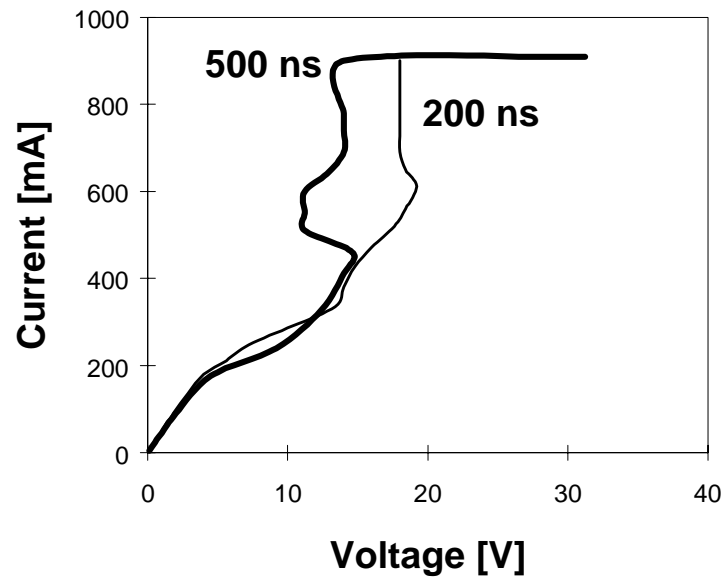
Resistor Design Option-II

nMOAT (Silicide Block)

$L/W = 25/5$



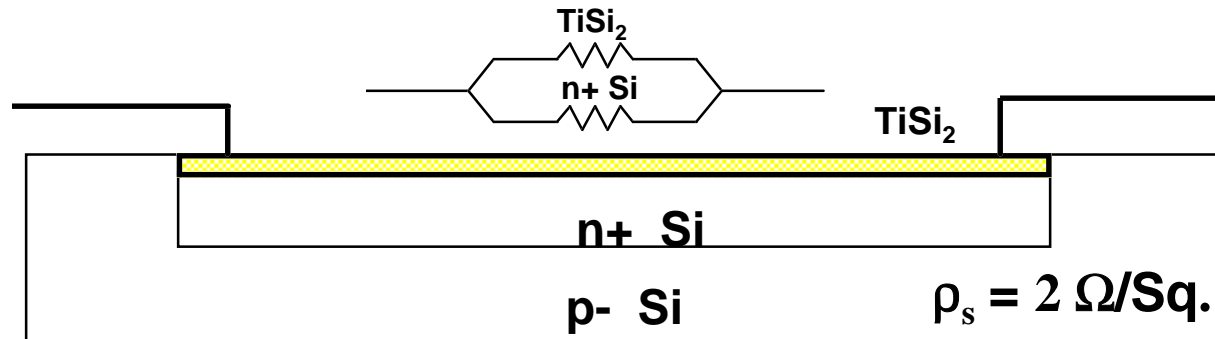
Transmission Line Pulsed Experiment



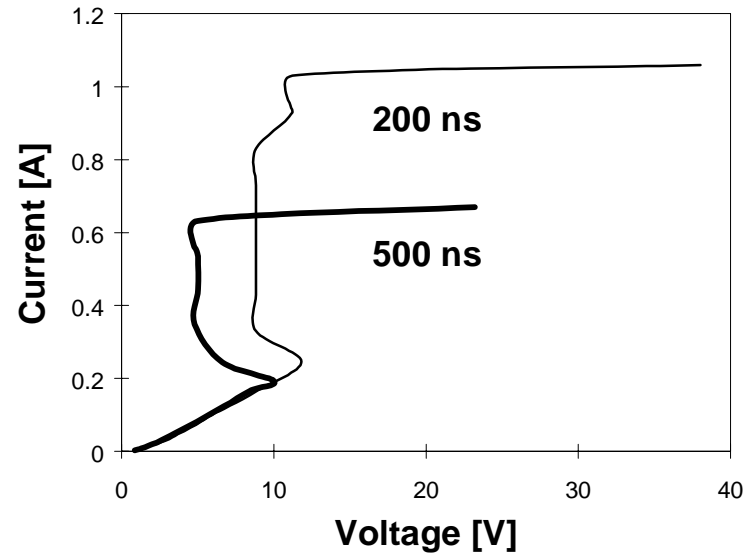
Resistor Design Option-III

nMOAT or
nContact

$L/W = 5/5$

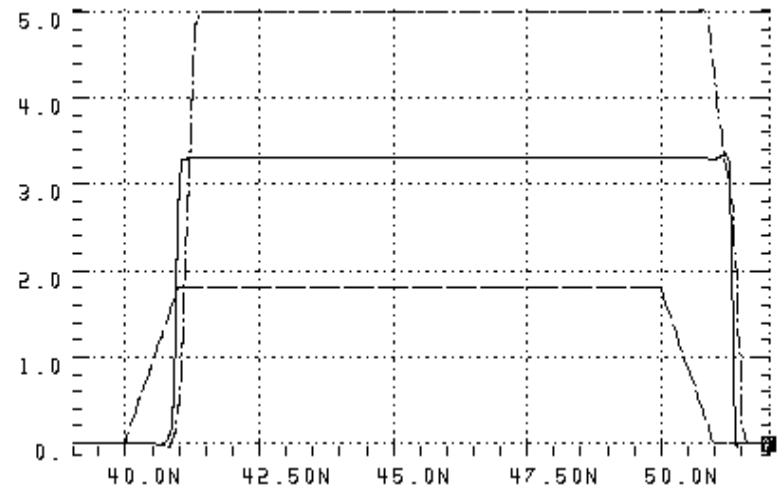
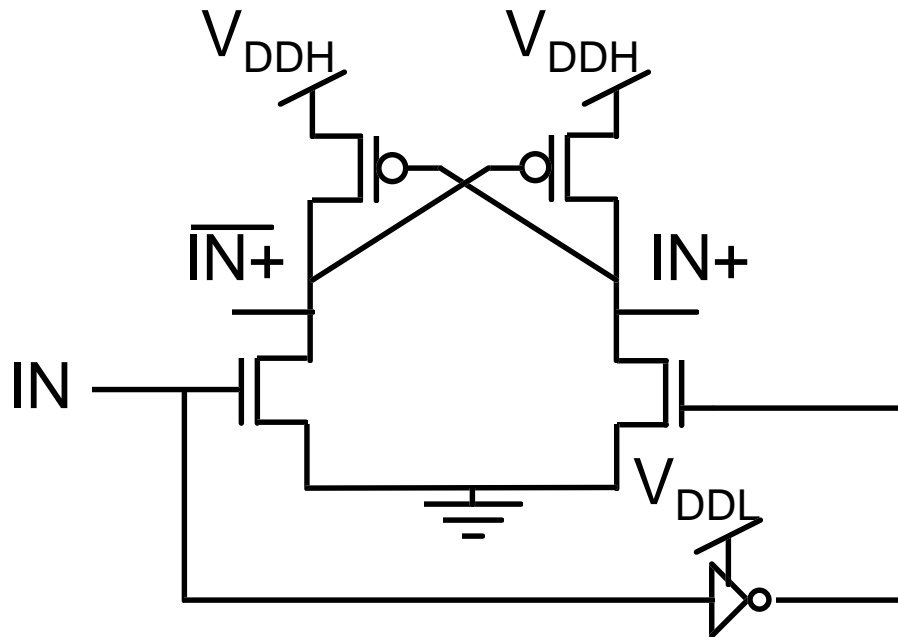


Transmission Line Pulsed
Experiment



Intra-Chip Buffers I

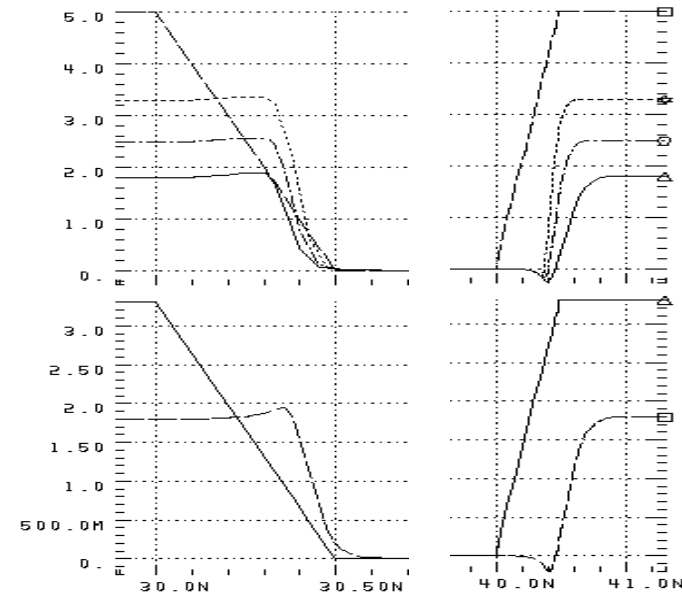
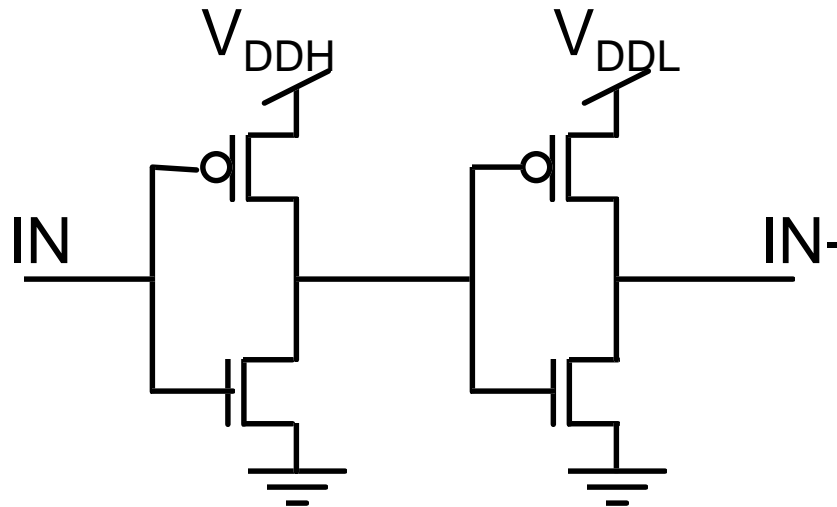
- Convert from lower voltage to higher voltage



- Size devices to ensure that positive feedback forces output to correct state for lowest possible input voltage

Intra-Chip Buffers II

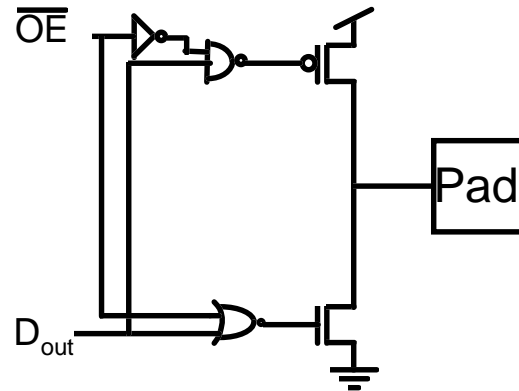
- Convert from higher voltage to lower voltage



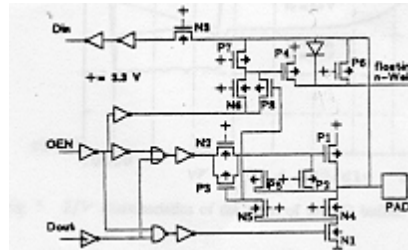
- Simple and easy
- When intermediate node is at V_{DDH} , PMOS device is turned fully off, ensuring accurate logic at output

Inter-Chip Buffers: Previous Implementations I

- Standard Output Buffer



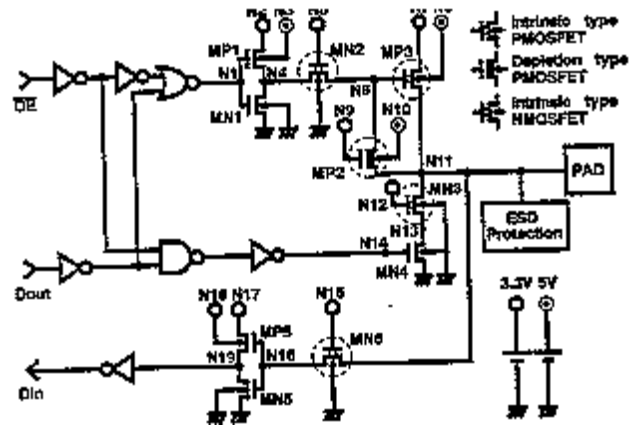
- Pelgrom '95 (JSSC)



- Drawbacks
 - Slow (~4 ns delay)
 - Circuitry in PMOS signal Path

Inter-Chip Buffers: Previous Implementations II

- Toshiba 1992 (CICC)

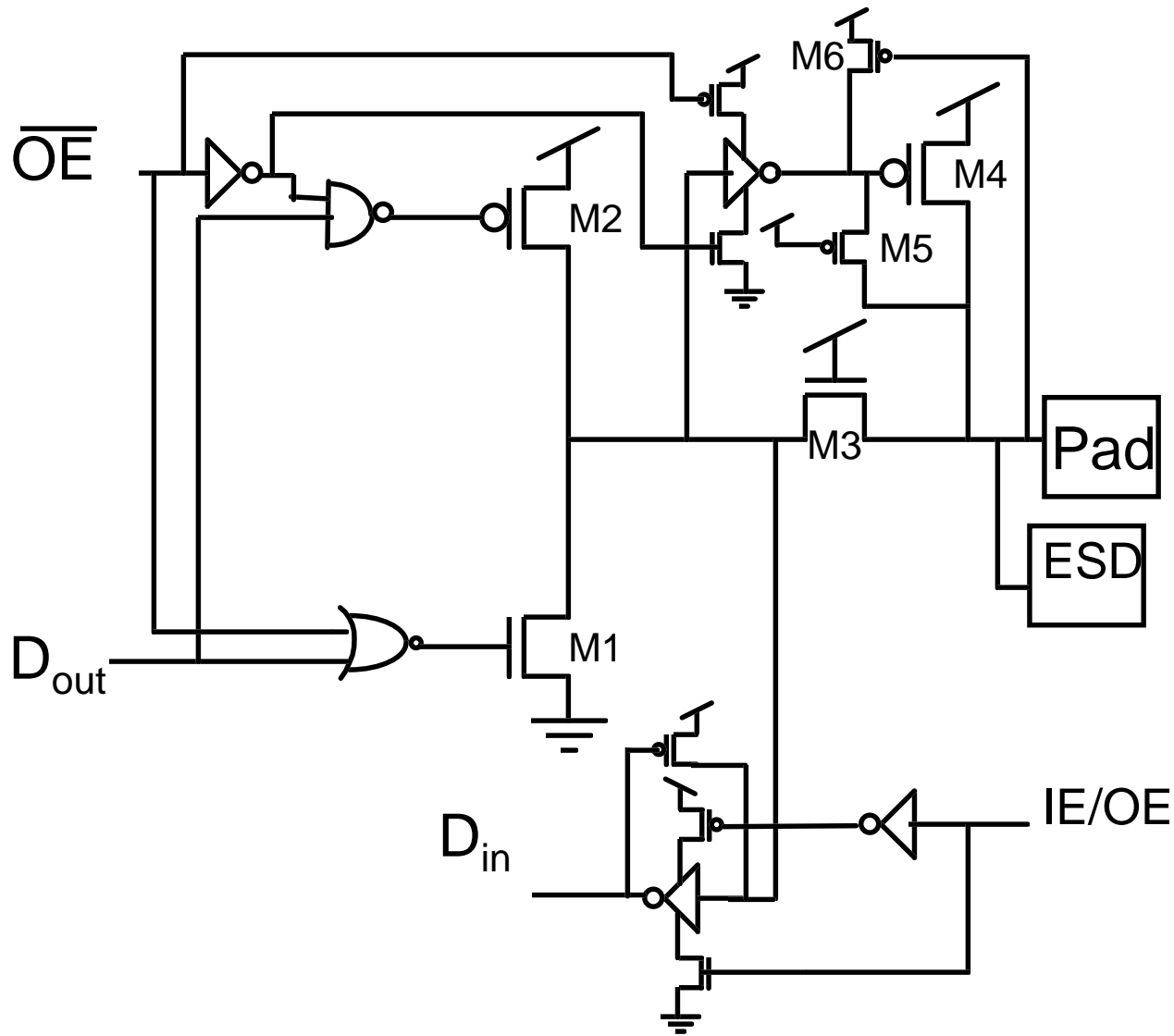


- Drawbacks
 - Slow (2.75 ns)
 - Depletion mode devices needed
 - Excessive circuitry in PMOS path

Goals of Output buffer circuit

- High Speed
- Limit number of devices in signal path
- Modular - minimize restrictions on voltages, etc.
- Minimize extra area

Inter-chip I/O Buffer Design



Design Issues and Benefits

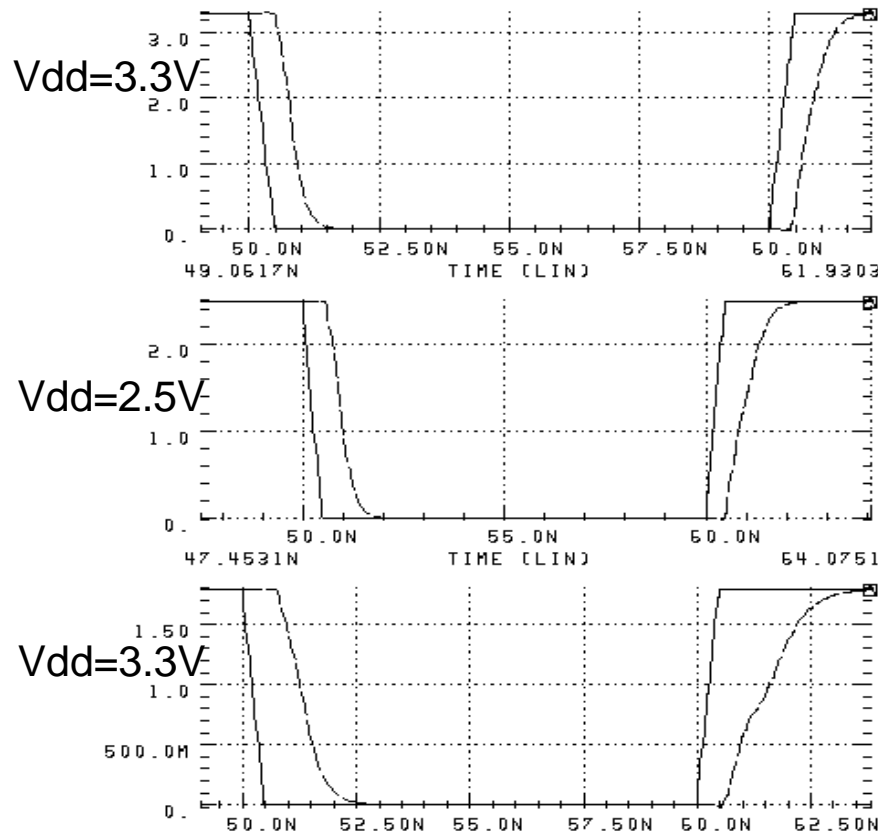
Benefits

- Really only ONE device between Inverter and Pad (PMOS pull-up there only for final V_{tn})
- Pass Transistors limit voltage across Gate Oxide to Chip V_{dd} or less
- Basic Buffer Stage Unchanged - additions are to output node, which is already driving a large capacitance
- Relatively Fast

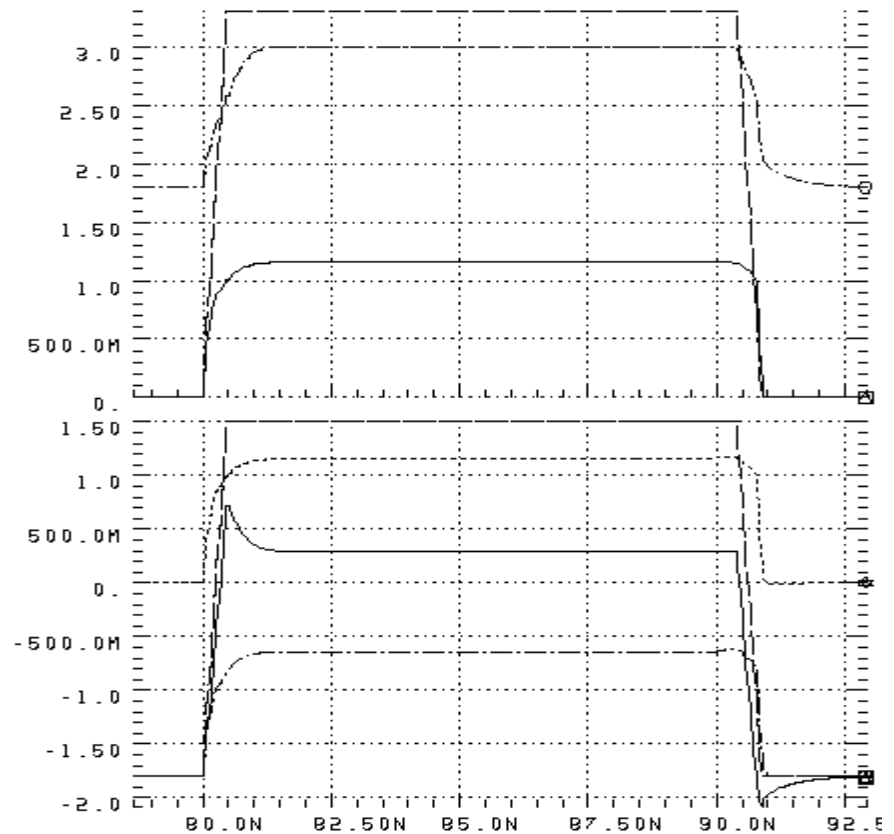
Sizing Issues

- Pass Transistor Size not too critical
- Size of PMOS devices at output limit low-high transition speed

Simulation Results



$t_p < 1.2 \text{ ns}$



All gate oxide voltages
less than 1.8V

Compare to previous Work

- **Pelgrom** - 0.8 μm and 0.6 μm - 5 ns delay
- **Toshiba** - 0.5 μm - 2.75 ns delay
- **This work** - 0.5 μm Post layout simulation
 - 1.1 ns delay (3.3-1.8)
 - 0.5 ns delay (5-3.3 V) buffer sizes will likely be smaller at 3.3 V, delay \uparrow
- Moreover, the 0.5 μm process was a 3.3 V process
 - A lower voltage process (i.e. a 1.8V process) will have thinner gate oxides and better performance at 1.8V

Design Limitations

- Highest V_{DD} limited to $2 \times \text{lowest } V_{DD}$
- **Area Penalty** - New Buffer takes ~50% more area according to layout in the HP 0.5 μm process
 - However, layout was not optimized - good layout could reduce the excess area to ~25%
- **Lowest V_{DD} Limited to $2 \times V_t$** - pass transistor necessitates that, at least for input part of buffer.
- Buffer **unable to convert to higher voltage** - hence other chips must be able to convert from lower voltage to communicate with this chip

Conclusions

- **New System of Buffers** for Multiple Power Supply Systems Demonstrated
- Intra-chip as well as Inter-chip buffers designed
- Buffers are of very **high speed and performance**
- **ESD protection** that accounts for higher supply voltages on different chips has been proposed