

A 1.9GHz 1W CMOS Class E Power Amplifier for Wireless Communications

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Abstract

A CMOS implementation of a Class E power amplifier for wireless communications which operates in the GHz region is reported. The concept of mode-locking is introduced in which the amplifier acts as an oscillator whose output is forced to run at the input frequency. A prototype was built, which delivered over 1W of output power with 48% power added efficiency, centred at 1.9GHz using a 2V supply.

1. Introduction

The proliferation of portable communication devices has generated a high demand for small and inexpensive transceivers with low power consumption. These desired characteristics can potentially be obtained through high levels of integration utilising a low-cost CMOS technology [1]. Typically, the dominant component of transceiver power consumption is the power amplifier (PA). The power added efficiency (PAE) of the PA,

$$PAE = \frac{\text{output power} - \text{input power}}{\text{supply power}}$$

is therefore one of the key figures of merit to optimise. The low breakdown voltage and low current drive of a typical CMOS transistor have made high efficiency PA implementations difficult using conventional approaches (e.g. Class A, B, AB and C). In addition, the efficiency of these conventional designs is typically optimised at the maximum output power which normally accounts for only a small portion of time in a transceiver's operation. For modern communication systems utilising constant envelope modulation, one attractive approach to alleviate these problems is to exploit the class of switching amplifiers such as the Class E power amplifier [2][3], which provides the potential of delivering high efficiency over a broad range of output power in a CMOS implementation.

Earlier realisations of CMOS PAs either provide low output power [4], or are implemented in a single-ended configuration which increases the possibility of coupling through the silicon substrate to other transceiver components, thus reducing the likelihood of full scale integration [5]. In addition, previously reported works

have been limited to operating frequencies below 1GHz. This paper describes a 1.9GHz fully differential CMOS power amplifier which can deliver over 1W of output power with higher PAE than previously published. This amplifier also operates on a low supply voltage, making it compatible with modern sub-micron, low-voltage VLSI technologies.

Section 2 will describe the basic operation and properties of a Class E amplifier, while section 3 and 4 provide descriptions of the design and implementation of a 1W, 1.9GHz CMOS PA. Experimental results are presented in section 5, followed by a brief conclusion in section 6.

2. Class E Amplifier

Power amplification of a constant envelope modulated signal can be achieved by extracting the fundamental component of a pseudo-periodic signal synchronised in phase and frequency with the input. Consider a simplified Class E PA in Fig.1. First we assume that the input toggles the switch periodically. When the switch is closed, a linearly increasing current is built up through the inductor. At the moment the switch is opened, this current is steered into the capacitor and causes the voltage across the switch, v_d , to increase. The tuned network is designed such that in steady state, v_d returns to zero when dv_d/dt is zero, immediately before the switch is closed again [6]. The bandpass filter then selectively passes the fundamental component of v_d to the load. In the case that v_{in} is phase or frequency modulated, the information embedded in the modulation is also passed to the output with a power amplification.

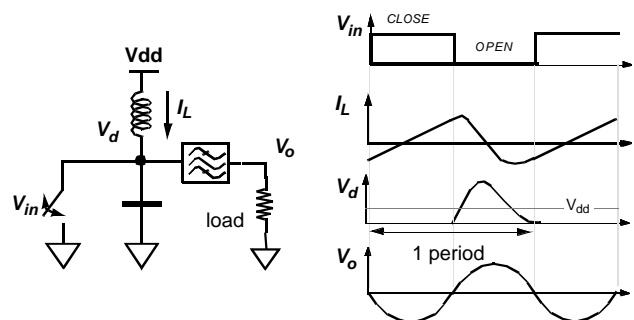


Fig.1. A simplified Class E PA and its steady state operation.

In principle, the voltage across the switch and the current through it are never simultaneously nonzero. Therefore, ideally the switch dissipates no power and all of the DC supply power is delivered to the RF output. Also, by design the capacitor is fully discharged at the moment the switch is closed and therefore no $\frac{1}{2}CV^2$ discharging energy is lost. This concept is commonly referred to as "soft switching."

In the case of a CMOS implementation, the soft switching nature of a Class E amplifier ensures that the MOS transistor is in the triode region when the switch is turned on, and hence acts as a simple resistor. This is in contrast to hard-switched switching amplifiers (e.g. Class D) where the transistor, during the turn-on transition, momentarily resides in the saturation region acting as a current source. The soft switching characteristic of a Class E PA allows it to be represented as being toggled between two linear LRC circuits as shown in Fig. 2.

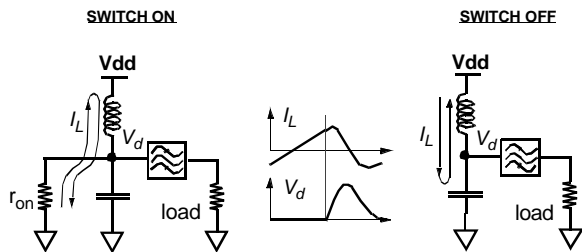


Fig.2. A Class E PA presented as switching between two linear LRC circuits.

Notice that current is not being actively drawn through the triode transistor when the switch is closed. Instead, current is being forced through the transistor by the inductor. Since the IR drop across the transistor is normally very small compared with V_{dd} , the exact value of r_{on} does not significantly affect the current circulation in the tuned load network. Therefore, quantities such as the output power are relatively insensitive to the detailed characteristics of the MOS transistor.

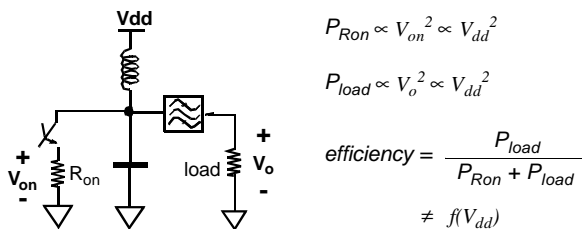


Fig.3. Loss and output power scaling with supply voltage.

Since the input voltage only provides timing information to the switch, the supply voltage becomes the only voltage reference in the circuit and voltages at all nodes are proportional to V_{dd} . This implies that the output power delivered to the load scales with V_{dd}^2 . As a result, output power control in a Class E PA can be effectively realised with a variable supply voltage implemented with a switching regulator. Such a power control scheme has an important advantage of maintaining a constant efficiency over a broad range of

output power. This is illustrated in Fig. 3 in which we assume, without loss of generality, that the only loss comes from the finite r_{on} of the switch. Since the loss and the output power both scale with V_{dd}^2 , their ratio, and the overall efficiency, is virtually unaffected as the output power is adjusted through the variable supply.

The simple circuit as described in Fig. 1 has a number of limitations in a GHz CMOS implementation. For instance, the size of the switching transistor is normally made as large as possible to reduce the loss due to the finite on-resistance. The input capacitor of this transistor is typically tuned out by an inductive load. However, beyond a certain transistor size the inductance values required to tune out the input capacitance may become too small to be realisable. In addition, the large C_{gd} of the transistor also induces strong output-input coupling. Finally, the single-ended circuit illustrated in Fig. 1 discharges a large current to ground, or the silicon substrate, once per cycle. This leads to an unwanted substrate coupling occurring at the same frequency as the desired input and output signals. These problems can be addressed by techniques detailed in the following section.

3. Design and Implementation

Fig. 4 shows a two-stage CMOS Class E power amplifier designed to operate in the GHz frequencies. A fully differential configuration was used to alleviate the problem of substrate coupling. In a fully differential configuration, current is being discharged to ground twice per cycle and the resulting coupling to substrate occurs at twice the signal frequency, reducing the interference with the desired signals. In addition, for the same supply voltage and output power, the current passing through each switch in a differential configuration is lower than that in its single-ended counterpart. This allows a smaller transistor to be used on each side without increasing the total switch loss. The differential configuration alone, however, does not provide sufficient size reduction for the transistors, especially because large on/off driving signals are required at their inputs. The technique of mode-locking is therefore introduced to solve this problem.

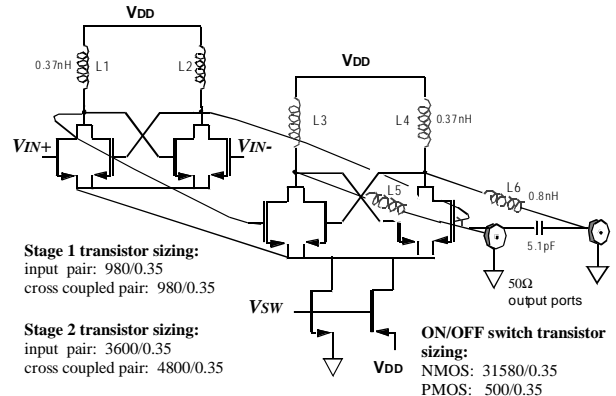


Fig.4. Schematic of the complete power Amplifier

Mode-locking technique: This refers to the condition in which an otherwise self-oscillating circuit is coupled and forced to run at the same frequency as an input signal, resulting in a substantial reduction in the input driving requirement. Mode-locking is realised in each stage of the amplifier by a pair of cross coupled devices as shown in Fig. 5. The two input voltages are out of phase, as are the two output voltages. The load impedance at the output nodes is designed such that v_{in1} and v_{o2} run in phase to control the composite switch. As far as each half circuit is concerned, the operation is similar to the single-ended version shown in Fig.1 with two main exceptions. First, the current originally circulating at each tuned load is now used to assist switching of the other half circuit. Second, the capacitance as seen at each input is much smaller for the same composite switch on-resistance. Like any other tuned circuit, a mode-locked amplifier can operate only within a certain frequency range. This locking range however, is reasonably large as verified by simulations and experiments.

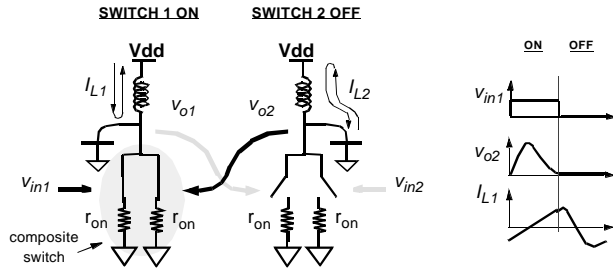


Fig.5. Illustration of the mode-locking concept.

Inductor realization: High Q inductors are critical in the design of high efficiency power amplifiers. This is especially true for a low voltage, high power design in which large currents circulate in the tuned network. Bondwires are used to realize such inductors. Bondwire inductance, however, is sensitive to bonding geometry and the existence of adjacent bondwires, making accurate predetermination of the inductance values difficult. Fortunately, once the configuration for a particular inductance value is known, it is rather repeatable in subsequent bondings. To realize the small inductance values shown in Fig. 4, short bondwires with currents running out of phase are placed adjacent to each other. As such, the effective inductance of each bondwire is reduced by the negative mutual inductance. Common bondwire metals include gold and aluminium. Gold is generally preferred because of its higher conductivity and flexibility. This allows higher Q bondwires with shorter physical lengths to be bonded for a given die height. The option of gold bondwire, however, is unavailable in the current implementation.

A pair of bondwires and an off-chip capacitor were used to realise an output matching network which matches each output to a 50Ω port. They also form a lowpass filter which performs a similar function as the bandpass filter in Fig. 1. An ON/OFF mechanism is

needed to prevent self-oscillation when the input signal is not available. This is conveniently implemented by inserting a switch between the common source and ground. Since the common source is a DC node, a very large switch can be used to ensure a low resistance to ground and to minimise series loss.

4. Experimental Prototype

A prototype circuit was fabricated in a $0.35\mu\text{m}$, single poly, 5 layer metal CMOS process. The chip area is $1.0\text{mm} \times 0.8\text{mm}$ including bonding pads. Assembly of the prototype device and the test board was done using a chip-on-board packaging technique in which the bare die was attached directly to the printed circuit board as shown in Fig. 6. The die was thinned to approximately $200\mu\text{m}$ before being attached to the ground plane with a conductive composite to facilitate heat dissipation and to reduce the minimum achievable bondwire length. Ground pads were "double bonded" to reduce parasitic ground inductance.

Aluminium bondwires of 1.25 mil diameter were used for bonding. After the drain and output bondwires were bonded, their inductance values were assessed by individual S-parameters measurements. Measurements were taken on adjacent bondwires in pairs so as to account for the effect of mutual inductance.

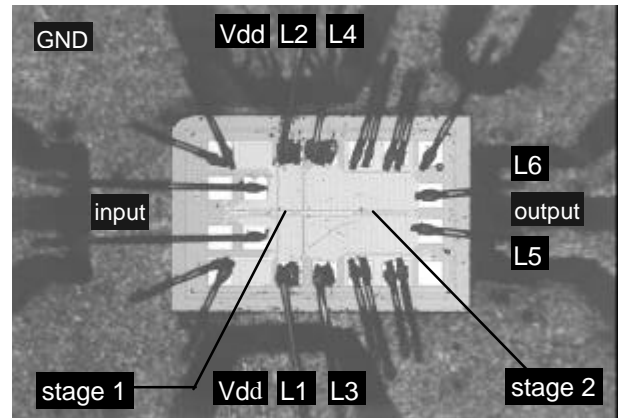


Fig.6. Chip-on-board assembly.

5. Measurement Results

A 10dBm single-ended input signal was converted to differential using an off-chip balun (Murata LDB20C500A1900) and then applied to the PA. RF power was measured across the 50Ω output ports. Fig. 7 shows a typical plot of output power and PAE versus V_{dd} . The output power increases from 49mW to 1.0W monotonically as the supply is swept from 0.6V to 2V, and is approximately proportional to V_{dd}^2 . Notice that the PAE remains close to its maximum value for most of the possible output power range. Reduction in the PAE for low output power is partly due to the constant input power being applied to the amplifier.

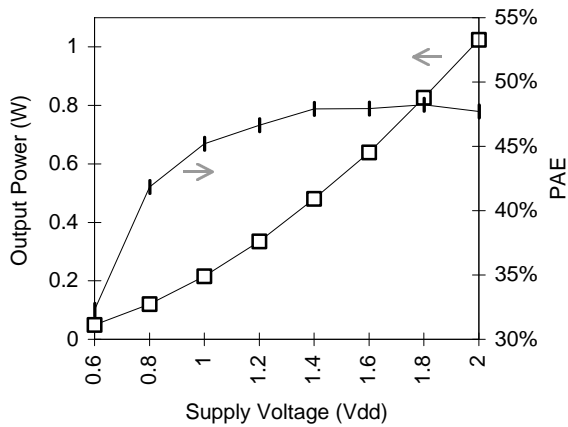


Fig.7. Output power and PAE vs. supply voltage. Frequency is 1.98GHz.

Fig. 8 shows the output power and efficiency at two different supply voltages across the range of input frequencies where the amplifier is mode-locked successfully. This locking range is measured to be about 500MHz, centring at about 1.9GHz.

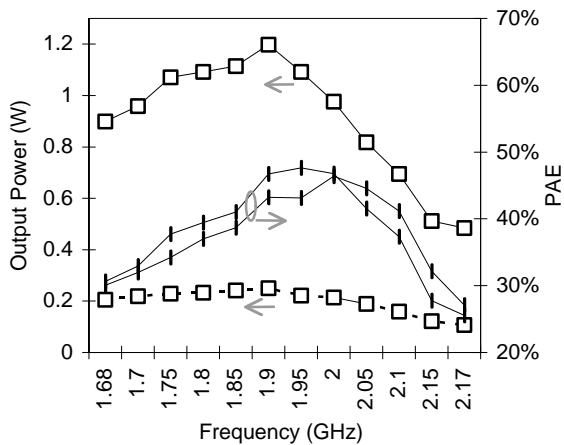


Fig.8. Output power and PAE vs. frequency. $V_{dd}= 1V$ (dotted) and $2V$ (solid).

In order to verify its potential in practical communication applications, the mode-locked Class E PA was tested with a Gaussian Minimum-Shift Keying (GMSK) modulated input signal. GMSK is a constant envelope modulation scheme in which information is carried in the phase variation of the signal, making it well suited to switch-mode power amplification. This scheme is used in cellular and cordless standards such as the Global System for Mobile Communications (GSM, BT=0.3) and the Digital European Cordless Telephone (DECT, BT=0.5.) The modulation parameter BT refers to the product of the Gaussian filter bandwidth and the symbol duration. As an example, a random bit sequence was modulated with BT=0.3 and the modulated signal was applied to the PA. The output spectrum, as shown in Fig. 9, shows no observable distortion and remains confined in the GSM spectral emission specifications.

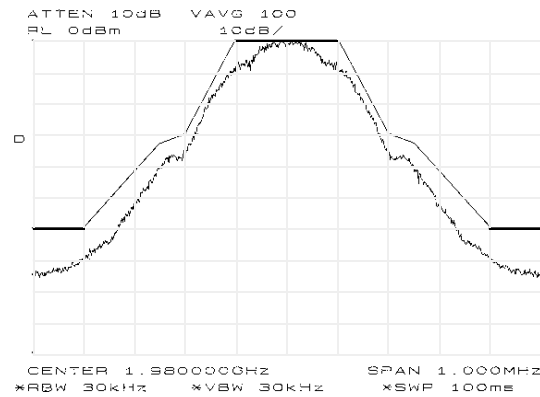


Fig.9. Amplified GMSK modulated signal (BT=0.3) and the GSM spectral emission mask.

6. Conclusion

A switch-mode Class E PA is suggested as an alternative to conventional approaches, for low-cost and high efficiency CMOS implementations. Differential topology and mode-locking technique are used to drive large switches with reduced substrate noise coupling. Potentials for modern communication systems are demonstrated from the measured power, efficiency and spectral performance.

7. Acknowledgement

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